

Compal Confidential

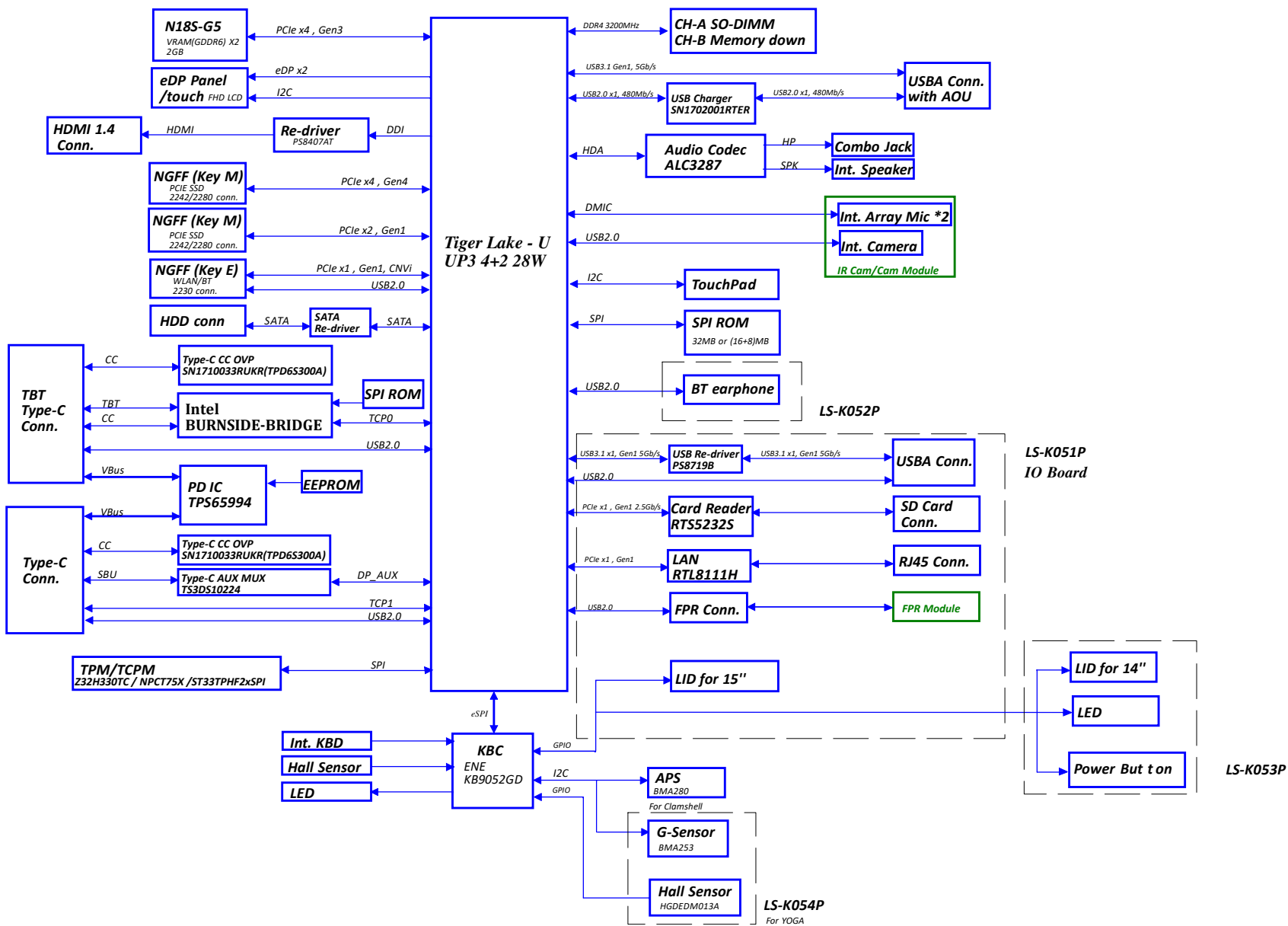
FLV34 GLV3Y MB Schematic Document

LA-K051P

Rev: 1.A

2020.07.21

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BOM Structure Table

Funct i on	Stuf f	Un-Stuf f
dGPU SKU	DIS@	UMA@
dGPU support GC6	GC6@	NOGC6@
YOGA SKU	YOGA@	CLAHSHELL@
CLAMSHELL SKU	CLAHSHELL@	YOGA@
DDR DDP	DDP@	SDP@
DDR SDP	SDP@	DDP@
EMI / ESD / RF Components	EMI@ RF@ ESD@ BT_EMI@	@EMI@ @RF@ @ESD@
CNVI	CNVI@	RMT@
CMC	CMC@	
SPI ROM	16+8M@	32M@
USBA AOU	AOU@	NAOU@
TPM	TPM@ ST@ /Nuvton@/ Nat i ons @	NTPM@
GLITCH	GLITCH@	
KB Backlight	KBL@	
Touch Screen	TOUCH@	@TOUCH@
For Signal Test	MP@	
BT earphoen	BT@	
HDD	HDD@	@HDD@
Finger Print	FP@	NFP@
NC Components	@	
ME Cnector	ME@ CLIP@	
JUMP (HW & PWR)	JUMP@	@JUMP@

HSIO Port Table (CPU)

HSIO Port	Capable	Port Allocat i on	PCIE CLK	NOTE
0	PCie4 #0	SSD1	CLK0 & CLKREQ#0	PCie interface
1	PCie4 #1			
2	PCie4 #2			
3	PCie4 #3			

HSIO Port Table (PCH)

HSIO Port	Capable	Port Allocat i on	PCIE CLK	NOTE
0	USB3.1 #1 / PCie #1	USB3.1 Type A Port 1 (MB)	NA	USB3.1 interface
1	USB3.1 #2 / PCie #2	USB3.1 Type A Port 2 (DB)	NA	USB3.1 interface
2	USB3.1 #3 / PCie #3	SSD2	CLK3 & CLKREQ#3	PCie interface
3	USB3.1 #4 / PCie #4			
4	PCie #5	dGPU	CLK4 & CLKREQ#4	PCie interface
5	PCie #6			
6	PCie #7			
7	PCie #8			
8	PCie #9	LAN	CLK1 & CLKREQ#1	PCie interface
9	PCie #10	Carder Reader	CLK2 & CLKREQ#2	PCie interface
10	PCie #11 /SATA0	HDD	NA	SATA interface
11	PCie #12 /SATA1	WLAN	CLK5 & CLKREQ#5	PCie interface

Power State

STATE	SIGNAL	SLP_S0#	CPU_C10_GATE#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)		HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		HIGH	HIGH	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		HIGH	HIGH	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Sof t Off)		HIGH	HIGH	LOW	LOW	LOW	ON	OFF	OFF	OFF
SOIX		LOW	LOW	HIGH	HIGH	HIGH	ON	ON	ON	ON

USB2.0 Port Table

USB2.0 Port	Device
1	USB Type-A (MB)
2	USB Type-C (MB TBT)
3	USB Type-C (MB)
4	BT earphone
5	USB Type-A (DB)
6	NA
7	RGB Camera
8	NA
9	Finger print
10	NGFF WLAN+BT (KEY E)

SOC SMBUS Address Table (TBC)

SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
SOC_SMBCLK SOC_SMBDATA	+3V_PRIM	DIMM1	TBC	TBC	0xA0
		DIMM2	TBC	TBC	0xA4
SOC_SML0CLK SOC_SML0DATA	+3V_PRIM	Re-Timer	TBC	TBC	TBC
SOC_SML1CLK SOC_SML1DATA	+3V_PRIM	PD (CYPD5225)	0x08h	TBC	TBC
		PD (TI65988)	TBC	TBC	TBC

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
EC_SMB_CK1 EC_SMB_DA1	+3VLP_EC	BAT	0x16	TBC	TBC
		CHGR	0x12	TBC	TBC
EC_SML1CLK EC_SML1DATA	+3VLP_EC				
		GPU	0x41	TBC	TBC
		THERMAL	0x4C	0X98	0x99
		PD (CYPD5225)	0x08h	TBC	TBC
		PD (TI65988)	TBC	0X46 0X4E	0X47 0X4F

I2C Address Table (TBC)

I2C Port	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
I2C 0	+3VS	G-Sensor KXCJ9-1008	0x0FH	TBC	TBC
		ALS CM32181A3OP	0x48H	TBC	TBC
I2C 2	+3VS	HDMI2.0 Re-Timer	TBC	TBC	TBC
I2C 3	+3VS	Track Pad	0x2CH	TBC	TBC
ISH_I2C 0	+1.8VS	SENSOR_KMX61G (Reserve)	0FH	TBC	TBC

Voltage Rails

Power Plane	Descript i on	S0	S0ix	S3	S4/S5
+20V_AD P_IN	Adapter power supply	N/A	N/A	N/A	N/A
+12.6V_BATT	Bat tery power supply	N/A	N/A	N/A	N/A
+19VB	AC or bat tery power rail f or power drcut	N/A	N/A	N/A	N/A
+VCCIN	Core voltage for CPU	ON	OFF	OFF	OFF
+VCCIN_AUX	CPU and PCH merged auxiliary power rail	ON	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF
+1.0VS_DGPU	+1.0VS power rail for GPU	ON	OFF	OFF	OFF
+1.05V_VCCST	Sustain voltage for CPU standby modes	ON	ON	ON	OFF
+1.05VS_VCCSTG	Gated sustain voltage for CPU standby modes	ON	OFF	OFF	OFF
+1.2V_VCCPLL_OD	+1.2V power rail for CPU digital PLL	ON	OFF	ON	OFF
+1.35VS_VRAM	+1.35VS power rail for GPU	ON	OFF	OFF	OFF
+1.2V_VDDQ	DDR4/L-RS +1.2V power rail	ON	ON	ON	OFF
+2.5V	DDR4/L-RS +2.5V power rail	ON	ON	ON	OFF
+1.8V_PRIM_SOC	TCSS/AGSH TypeC sub system / CPU analog power supply	ON	OFF	OFF	OFF
+1.8VALW	System +1.8V power rail	ON	ON	ON	ON*
+1.8VS	System +1.8VS power rail	ON	ON	OFF	OFF
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*
+3V_PRIM	+3VALW power for PCH suspend rails	ON	ON	ON	ON*
+3VS	System +3VS power rail	ON	ON	OFF	OFF
+1.8VS_DGPU_AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VS_DGPU	+1.8VS power rail for GPU	ON	OFF	OFF	OFF
+VGA_CORE	Power rail for GPU	ON	OFF	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON	ON*
+5VS	System +5VS power rail	ON	ON	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

Load BOM Option Table

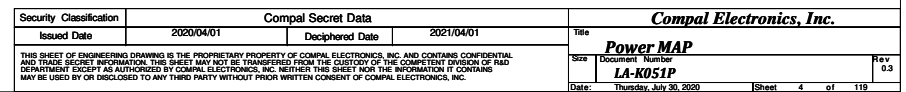
BOM Number	Load BOM Option
431ACX30L01(DISCRETE)	
431ACX30L02(UMA)	

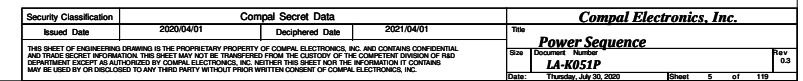
Load BOM Option Table for Baseline

BOM Number	Load BOM Option
431ACX30L01(DISCRETE)	
431ACX30L02(UMA)	

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EOA01 Schematic: 1A-H591P001 0401A





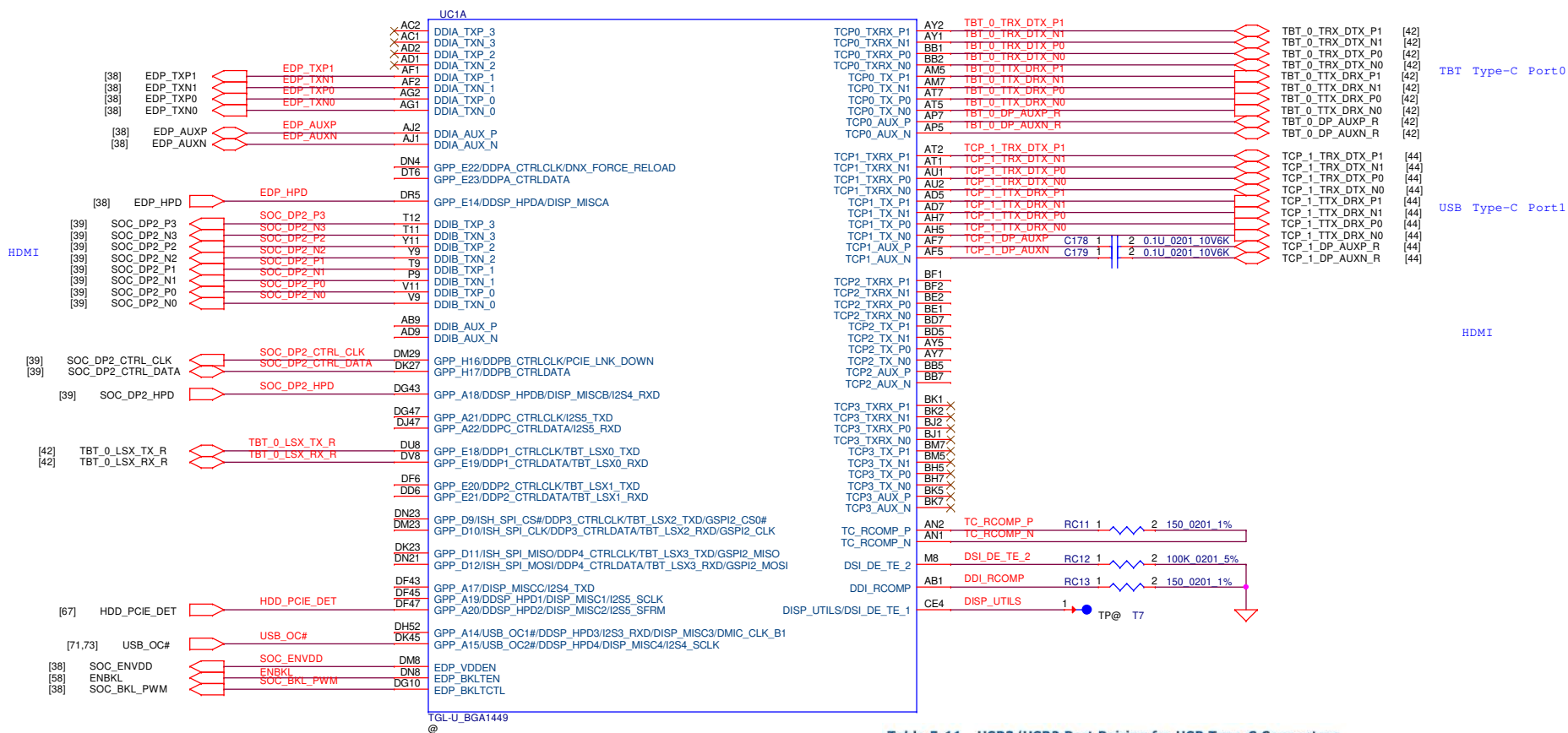
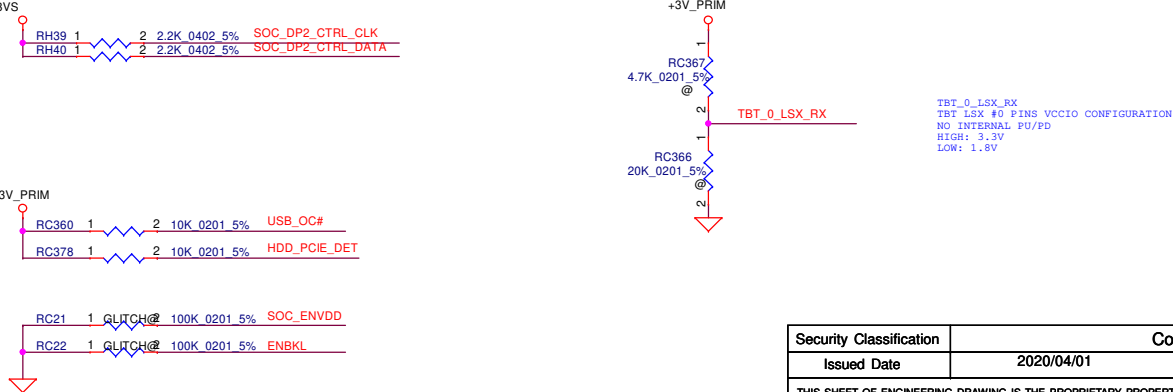


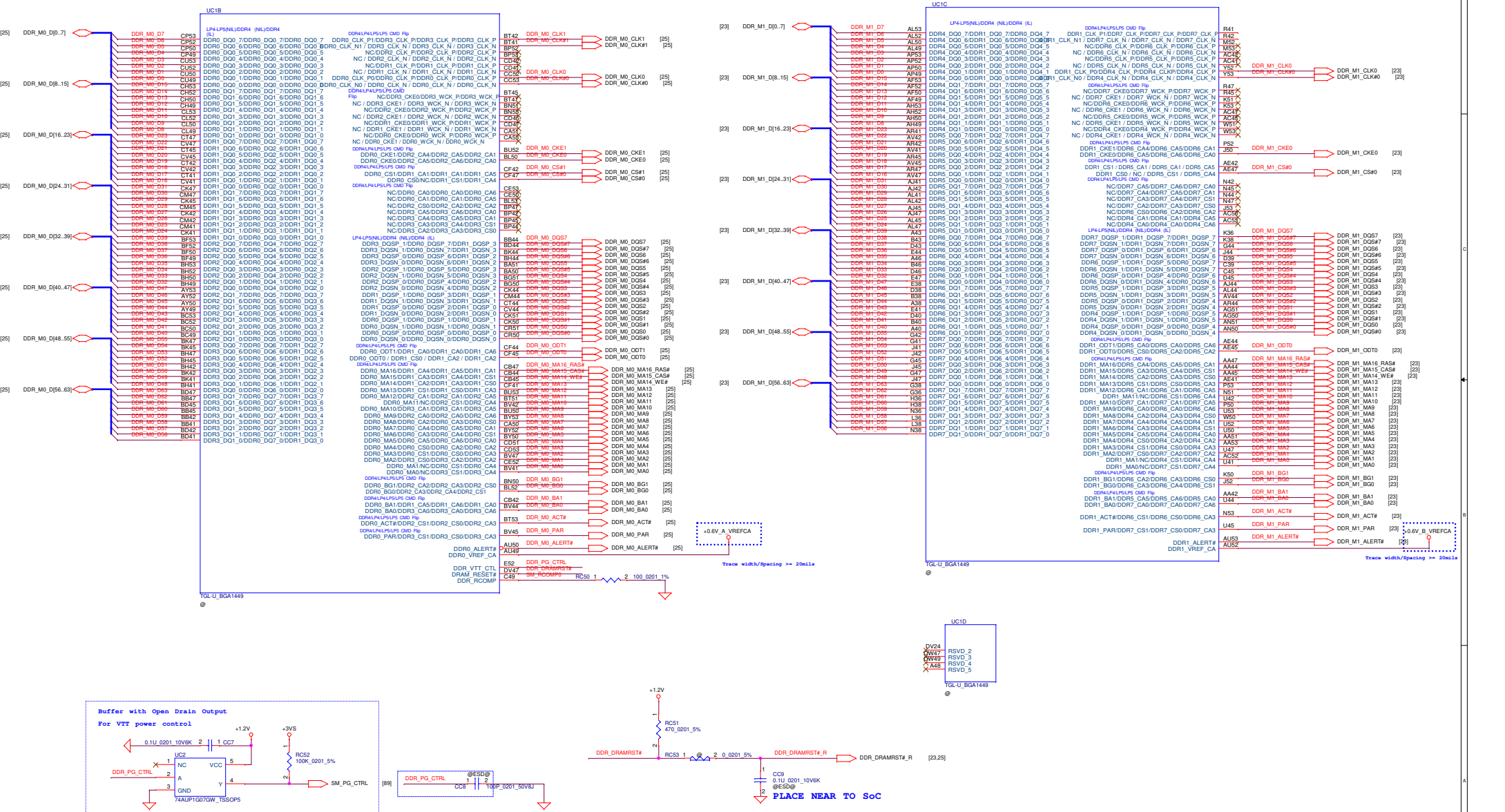
Table 5-11. USB3/USB2 Port Pairing for USB Type-C Connectors

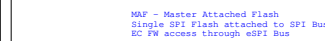
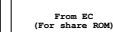
	Connector C0	Connector C1	Connector C2	Connector C3
CPU USB3 port#	1	2	3	4
PCH USB2 port#	2	3	4	6

To make split xDCI controller working functionally for different USB-C connectors with increasing port numbers (TCP0_*, TCP1_*, TCP2_*, TCP3_*), recommended to pair with increasing number of USB2 ports from PCH. Simplest form of requirement is to match USB2/USB3 port numbers for USB-C connectors, but it is not strictly required.

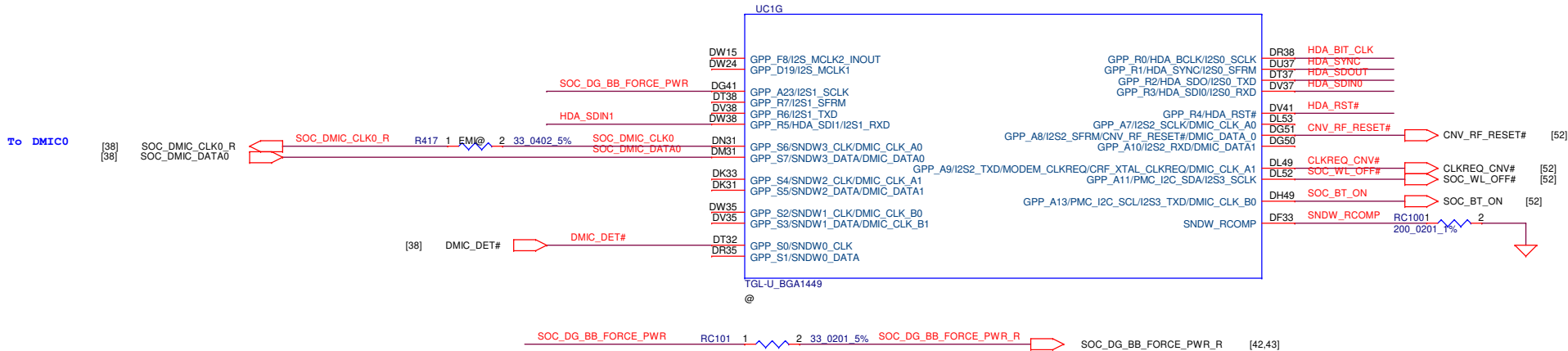


Follow Intel DDR4 N1L

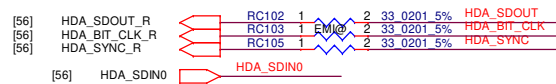




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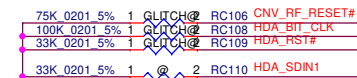
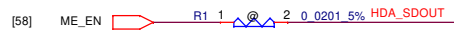


HDA for AUDIO



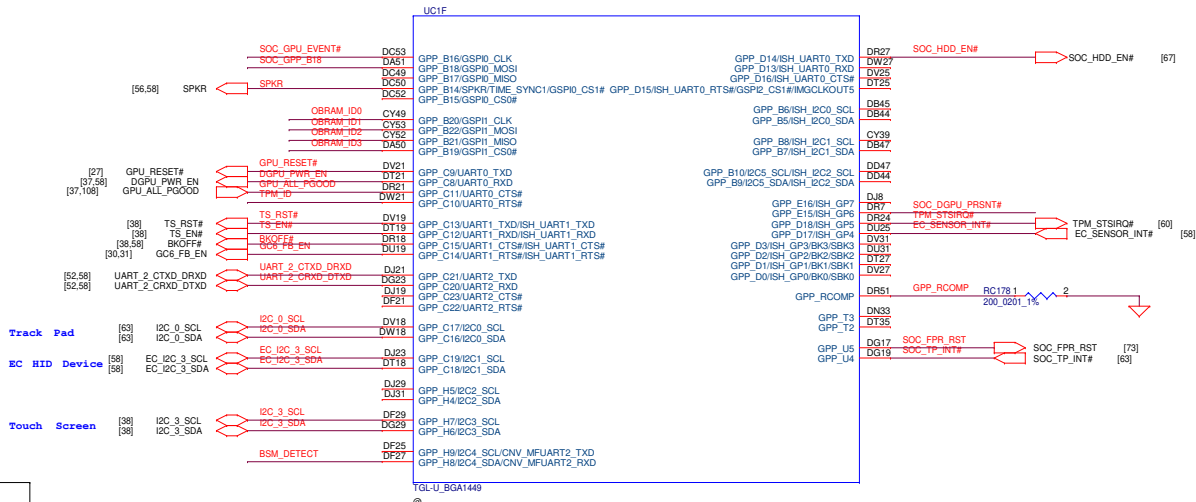
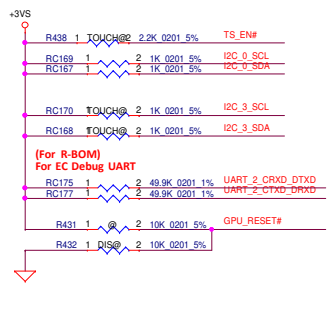
To Enable ME Override

HDA_SDOUT
FLASH_DESCRIPTOR SECURITY OVERRIDE
INTERNAL PD 20K
HIGH: OVERRIDEN
LOW: SECURITY MEASURES NOT OVERRIDEN (DEFAULT)



Follow
607872_TGL_UY_PDG for Glitch

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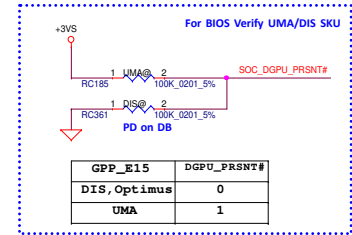
Track Pad

EC HID Device

Touch Screen

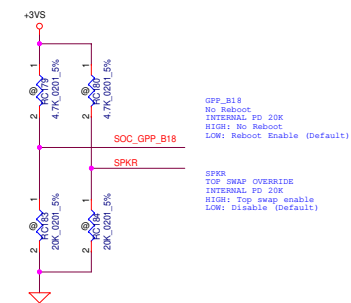
GPP_H8	Status
BattSaveMode Enable	0
BattSaveMode disable	1

GPP_C10	Status
TPM Stuff	1
TPM un-Stuff	0



GPP_E15	DGPU_PSRNT#
DIS,Optimus	0
UMA	1

Strap Pin



to dGPU Connect to SOC GPIO



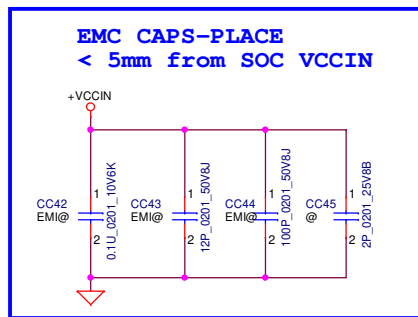
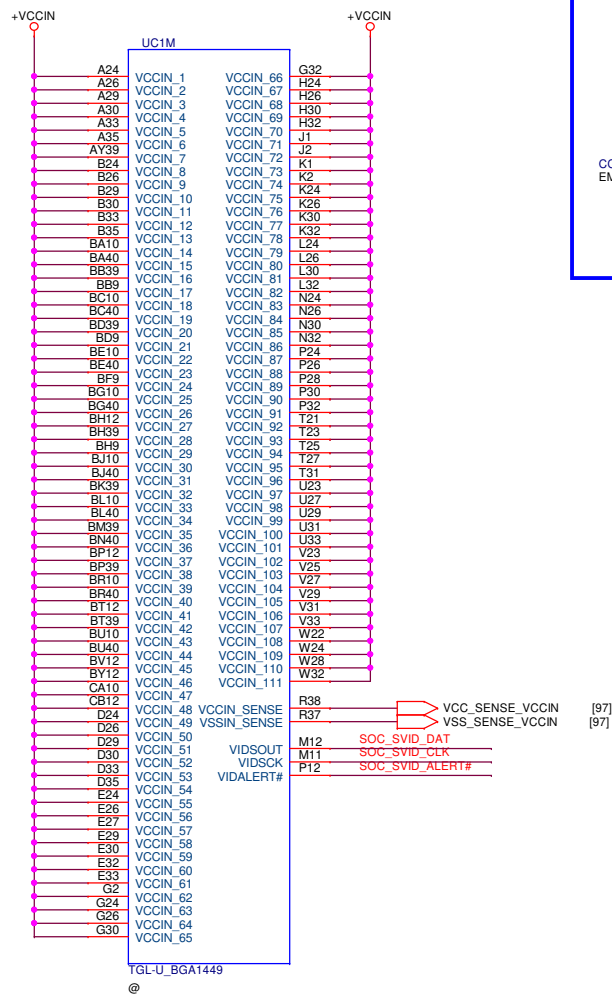
place the same side(TOP/BOT) with on board RAM IC

Capacity	Description	OBRAM_ID3	OBRAM_ID2	OBRAM_ID1	OBRAM_ID0	BOM Structure
4GB	WITHOUT ON-BOARD RAM	L	L	L	L	NO_MD@
	MT40A512M16T8-062E-J	L	L	L	H	DDR_M4G@
	HYNIX_H5AN8G6NCJR-XNC	L	L	H	L	DDR_H4G@
8GB	SAMSUNG_K4A8G165WC-BCWE	L	L	H	H	DDR_S4G@
	MICRON_MT40A512M16T8-062E-J	L	H	L	L	DDR_M8G@
	Samsung_K4AAG165WA-BCWE	L	H	H	L	DDR_H8G@

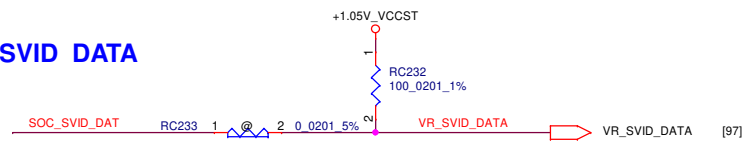
ON BOARD RAM

UD1_DDR_M4G@ MT40A512M16T8-062E-J SA0000C2500	UD2_DDR_M4G@ MT40A512M16T8-062E-J SA0000C2500	UD3_DDR_M4G@ MT40A512M16T8-062E-J SA0000C2500	UD4_DDR_M4G@ MT40A512M16T8-062E-J SA0000C2500
UD1_DDR_H4G@ HSAN8G6NCJR-XNC SA0000C2300	UD2_DDR_H4G@ HSAN8G6NCJR-XNC SA0000C2300	UD3_DDR_H4G@ HSAN8G6NCJR-XNC SA0000C2300	UD4_DDR_H4G@ HSAN8G6NCJR-XNC SA0000C2300
UD1_DDR_S4G@ K4A8G165WC-BCWE SA0000C2500	UD2_DDR_S4G@ K4A8G165WC-BCWE SA0000C2500	UD3_DDR_S4G@ K4A8G165WC-BCWE SA0000C2500	UD4_DDR_S4G@ K4A8G165WC-BCWE SA0000C2500
UD1_DDR_M8G@ MT40A512M16T8-062E-J SA0000C3U00	UD2_DDR_M8G@ MT40A512M16T8-062E-J SA0000C3U00	UD3_DDR_M8G@ MT40A512M16T8-062E-J SA0000C3U00	UD4_DDR_M8G@ MT40A512M16T8-062E-J SA0000C3U00
UD1_DDR_H8G@ HSAN8G6NCJR-XNC SA0000C2100	UD2_DDR_H8G@ HSAN8G6NCJR-XNC SA0000C2100	UD3_DDR_H8G@ HSAN8G6NCJR-XNC SA0000C2100	UD4_DDR_H8G@ HSAN8G6NCJR-XNC SA0000C2100
UD1_DDR_S8G@ K4AAG165WA-BCWE SA0000C2200	UD2_DDR_S8G@ K4AAG165WA-BCWE SA0000C2200	UD3_DDR_S8G@ K4AAG165WA-BCWE SA0000C2200	UD4_DDR_S8G@ K4AAG165WA-BCWE SA0000C2200

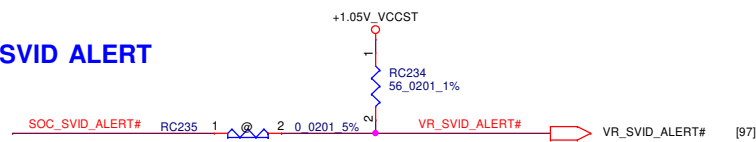
RC193_NO_MD@ 10K_0402_5%	RC192_NO_MD@ 10K_0402_5%	RC191_NO_MD@ 10K_0402_5%	RC190_NO_MD@ 10K_0402_5%
RC193_DDR_M4G@ 10K_0402_5%	RC192_DDR_M4G@ 10K_0402_5%	RC191_DDR_M4G@ 10K_0402_5%	RC186_DDR_M4G@ 10K_0402_5%
RC193_DDR_H4G@ 10K_0402_5%	RC192_DDR_H4G@ 10K_0402_5%	RC187_DDR_H4G@ 10K_0402_5%	RC190_DDR_H4G@ 10K_0402_5%
RC193_DDR_S4G@ 10K_0402_5%	RC192_DDR_S4G@ 10K_0402_5%	RC187_DDR_S4G@ 10K_0402_5%	RC186_DDR_S4G@ 10K_0402_5%
RC193_DDR_M8G@ 10K_0402_5%	RC188_DDR_M8G@ 10K_0402_5%	RC191_DDR_M8G@ 10K_0402_5%	RC190_DDR_M8G@ 10K_0402_5%
RC193_DDR_H8G@ 10K_0402_5%	RC188_DDR_H8G@ 10K_0402_5%	RC191_DDR_H8G@ 10K_0402_5%	RC186_DDR_H8G@ 10K_0402_5%
RC193_DDR_S8G@ 10K_0402_5%	RC188_DDR_S8G@ 10K_0402_5%	RC187_DDR_S8G@ 10K_0402_5%	RC190_DDR_S8G@ 10K_0402_5%



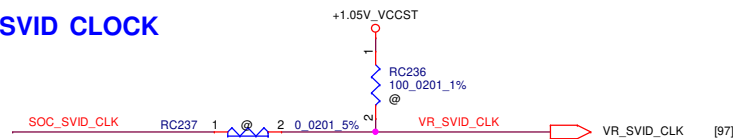
SVID DATA



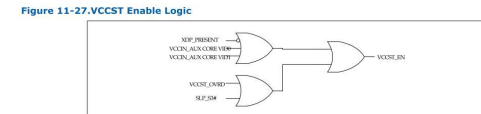
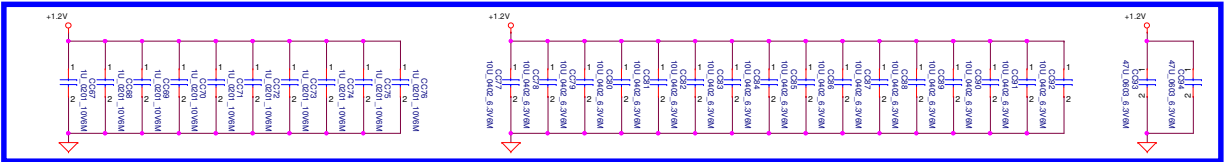
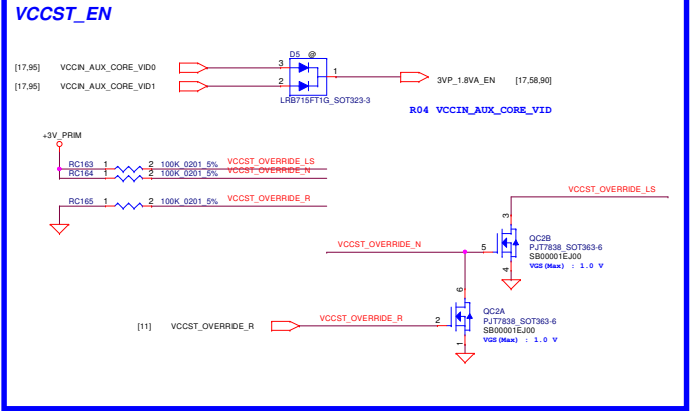
SVID ALERT



SVID CLOCK



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Singal Name		Input			
Framium	VCCIN_AUX_CORE_VID	H	D	D	L
	VCCST_CV_OVERRIDE_LS	D	H	D	L
	PM_SLP_S3# (SUSP#)	D	D	H	L
	EC_VCCST_EN Output	H	H	H	L
Volume	VCCIN_AUX_CORE_VID	H	D	D	L
	VCCST_CV_OVERRIDE_LS	D	H	D	L
	PM_SLP_S4# (SYSON)	D	D	H	L
	EC_VCCST_EN Output	H	H	H	L

Follow
609003_TGL_U_DDR4_SODIMM_RVP_SCH_REV0p5

I62 TP@ 1

TGL-U_BGA1449
@

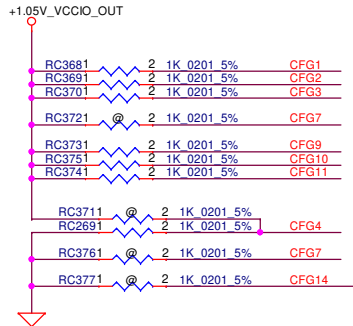
UC1Q

TGL-U_BGA1449
@

UC1R

TGL-U_BGA1449
@

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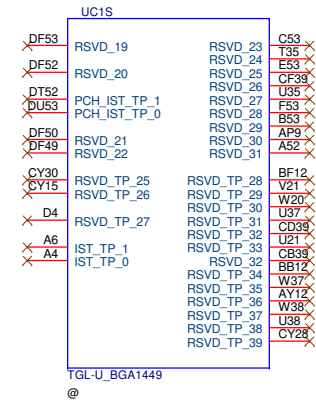
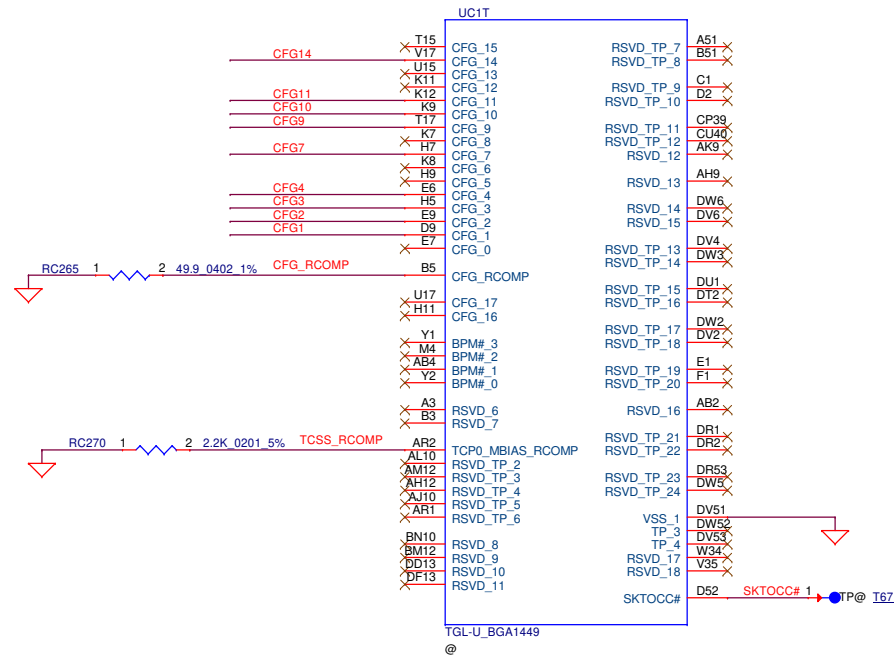


CFG4
Display port presence strap
LOW : Enable
An external display port device is connected to
the embedded displayport
HIGH : Disable
No physical display port attached to embedded display port

CFG7
PEG Training
LOW : PEG Wait for BIOS for training.
HIGH : (default) PEG Train immediately following
RESET# de assertion.

CFG14
PEG60 Lane Reversal
HIGH : (Default) Normal
LOW : Reversed

CFG	Description	Termination	Resistor
	Operation; No stall. - 0 = Stall		
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled, - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[1 7:15]	RSVD	None	



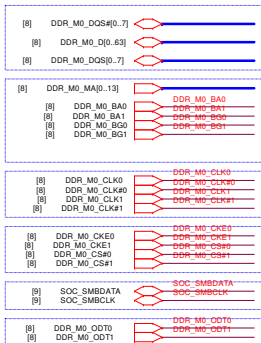
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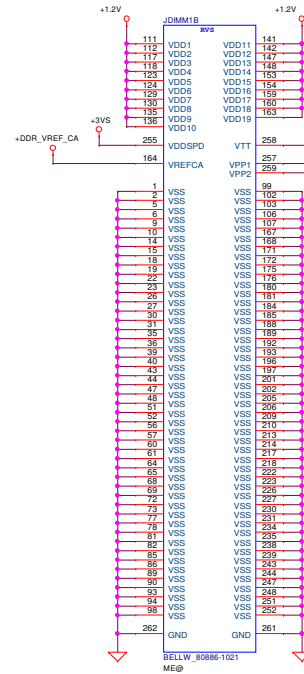
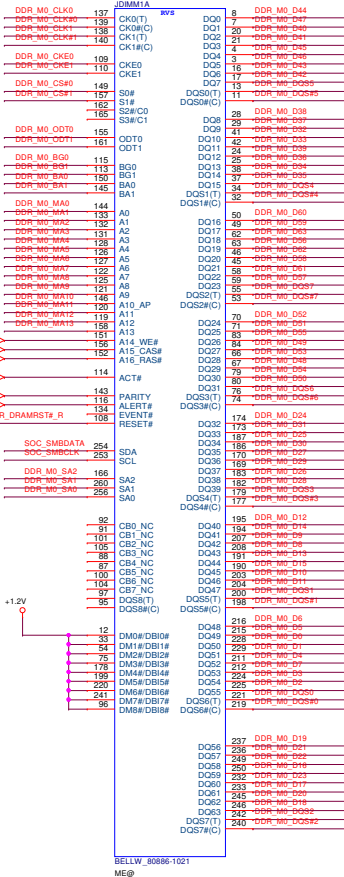
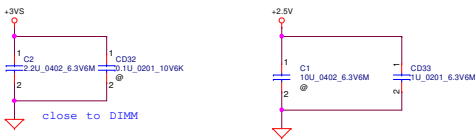
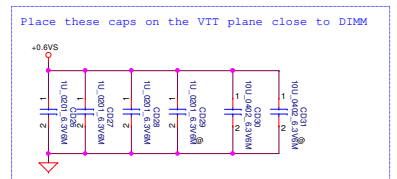
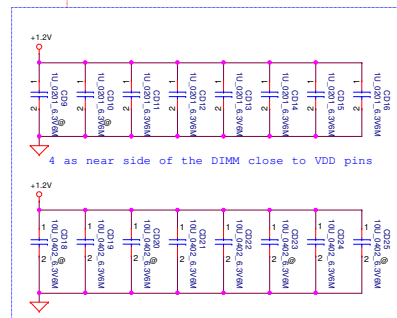
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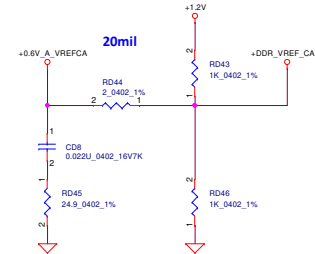
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Layout Note:
Place near JDIMM1

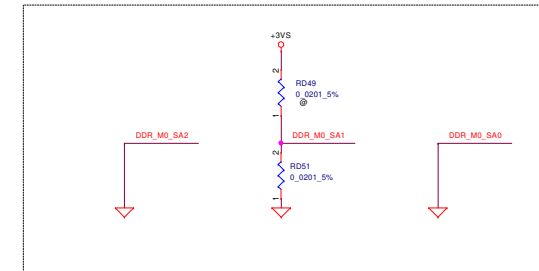


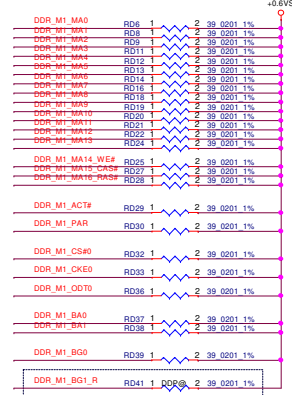
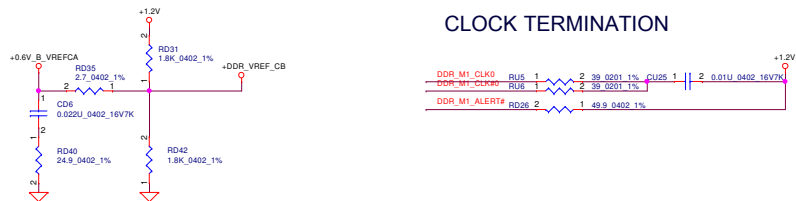
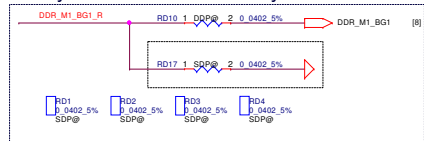
Standard Type
2-3A to 1 DIMMs/channel



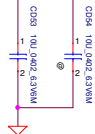
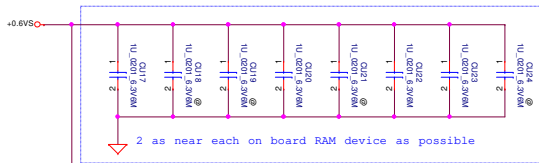
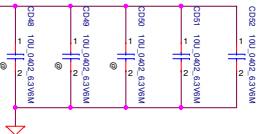
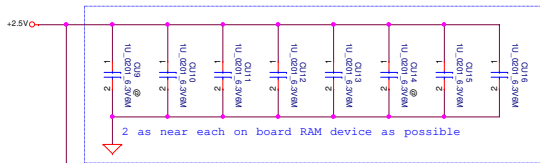
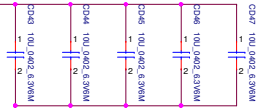
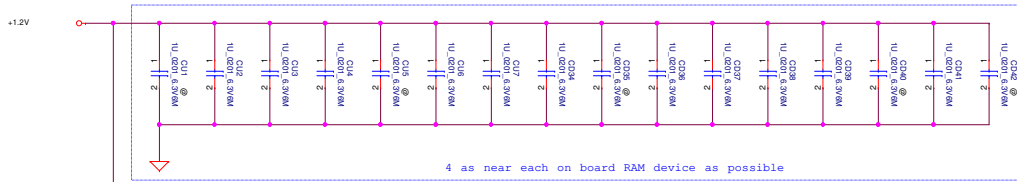
Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

JDIMM1 ADDRESS (PLACE CLOSE TO DIMM)





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GPU

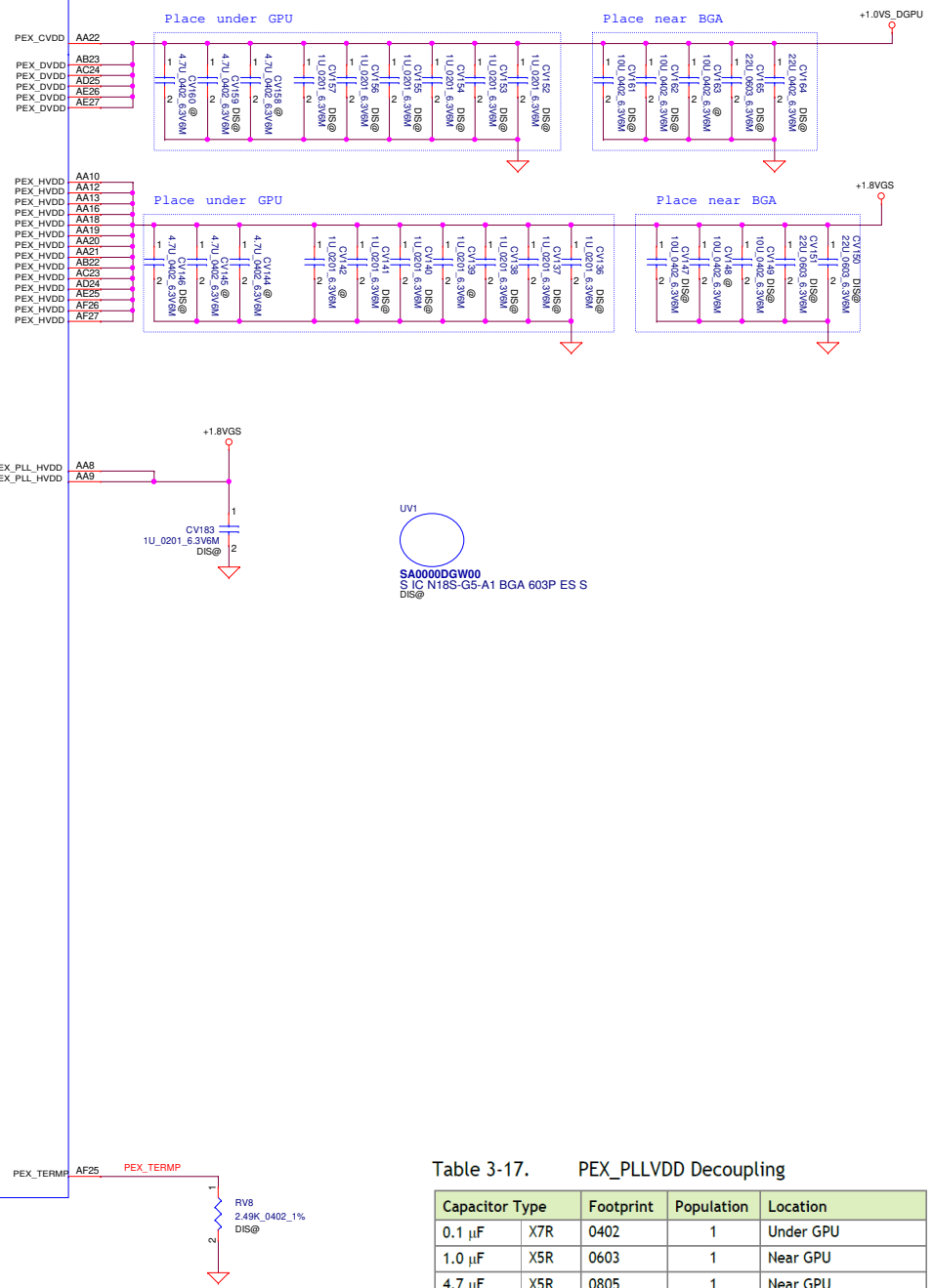
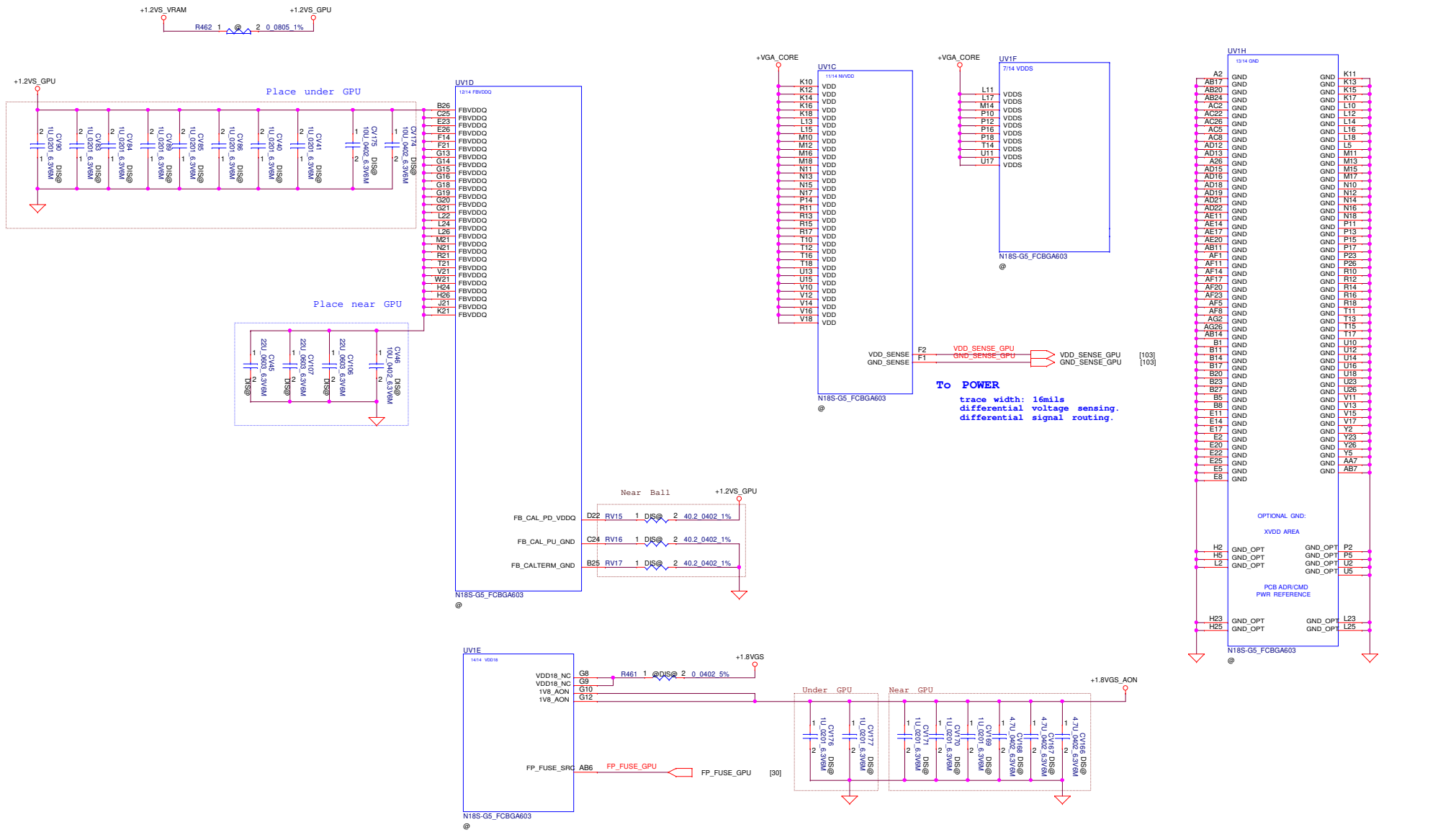
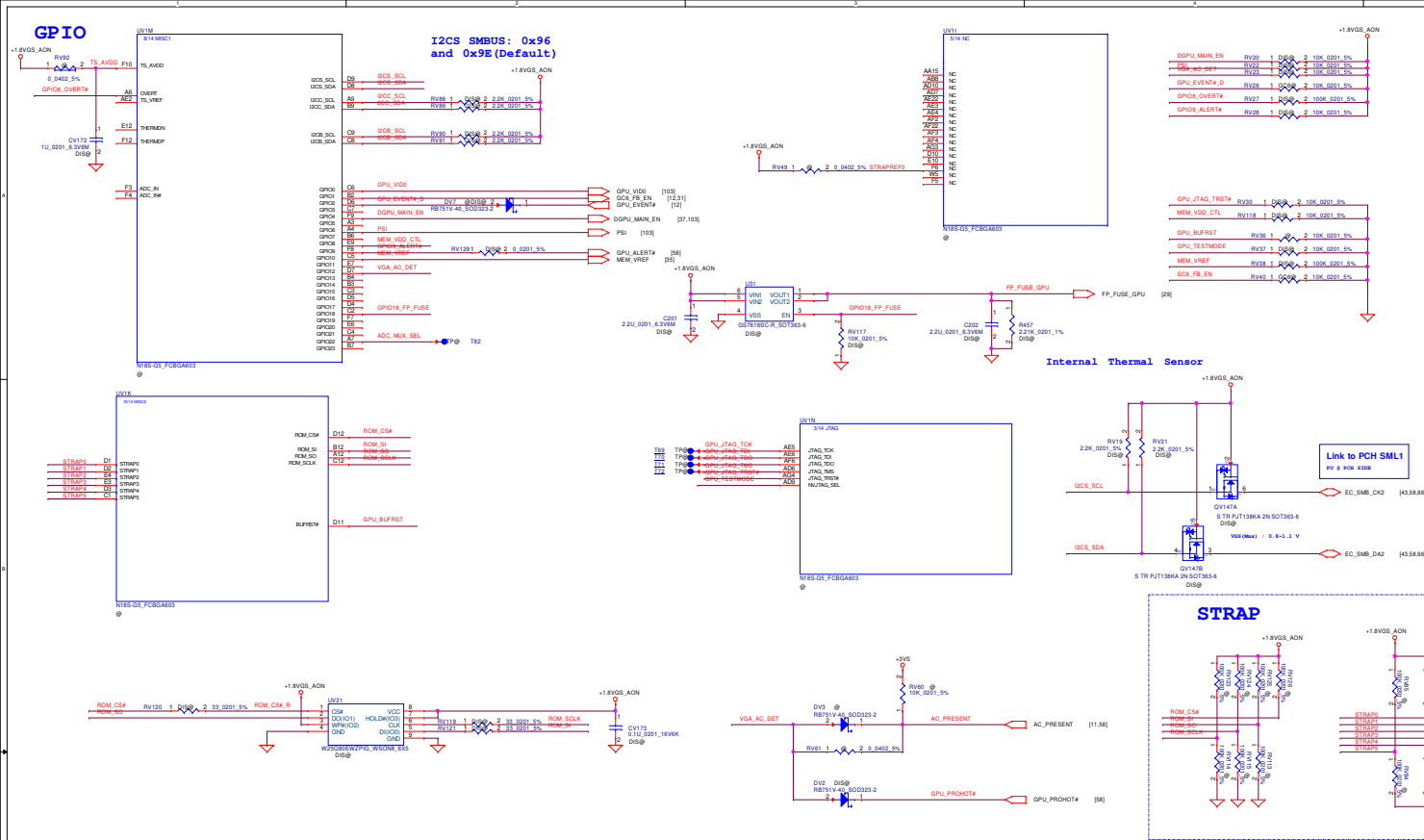


Table 3-17. PEX_PLLVDD Decoupling

Capacitor Type		Footprint	Population	Location
0.1 μ F	X7R	0402	1	Under GPU
1.0 μ F	X5R	0603	1	Near GPU
4.7 μ F	X5R	0805	1	Near GPU





N18S-G5 VRAM Strap

RAM_CFG	STRAP2	STRAP1	STRAP0	NOTE
0x1 MT61K256M32J-14:1A				
0x0 K4280325BC-HC14				

GPU	Memory Type	FBVDD/ FBVDDQ	Memory Density	Memory configuration	Vendor	Manufacturer Part Number	Die Revision	Memory Speed CK Grade	Memory D/C Minimum	Strap2	Strap1	Strap0	Status
N18S-G5	GD0R6	1.20V	8Gb	2chx256Mx16	Micron	MT61K256M32J-14A	A-die	14 Gbps	1940	0x1	L	L	H Production Candidate
					Samsung	K4280325BC-HC14	C-die	14 Gbps	2001	0x0	L	L	L Production Candidate

N18S Strap

	ROM_SI	ROM_SO	ROM_SCLK	STRAP3	STRAP4	STRAP5
Strap						

Item	N18S-G5	MS-hybrid Mode
Device ID	Primary: Secondary: N/A	
Package	GB2E-64	
Internal P/N		
ROM_SCLK (LSB)	1.BOM Option for 100K PU to 1V8_AON 2.BOM Option for 100K PD to GND	L
ROM_SI	1.BOM Option for 100K PU to 1V8_AON 2.BOM Option for 100K PD to GND	L
ROM_SO (MSB)	1.BOM Option for 100K PU to 1V8_AON 2.BOM Option for 100K PD to GND	L
Strap0 (LSB)	Refer to N18x_RAM_Straps table	
Strap1 (MSB)		
Strap2 (LSB)		
Strap3 (LSB)	1.BOM Option for 100K PU to 1V8_AON 2.BOM Option for 100K PD to GND	L
Strap4	1.BOM Option for 100K PU to 1V8_AON 2.BOM Option for 100K PD to GND	L
Strap5 (MSB)	1.BOM Option for 100K PU to 1V8_AON 2.BOM Option for 100K PD to GND	L
Boot Voltage	0.8V	

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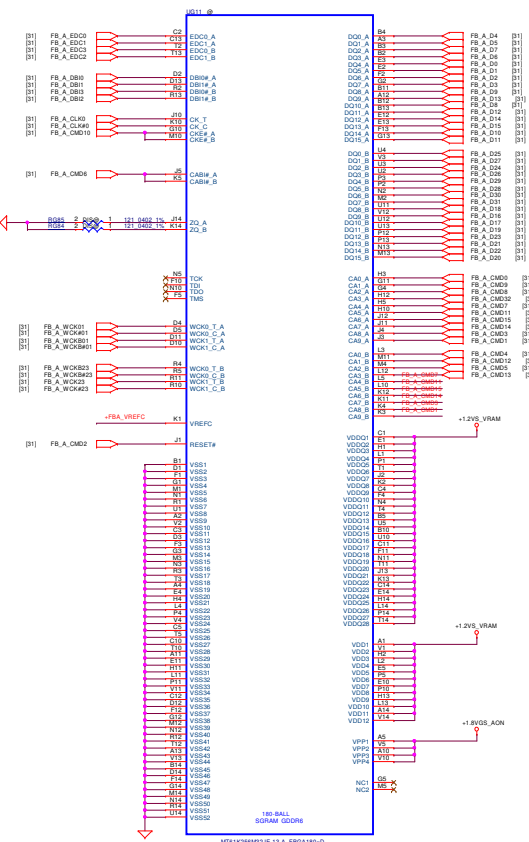
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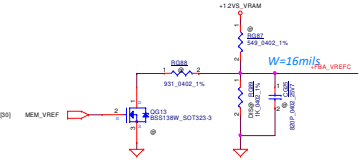
VRAM A

VRAM A Mapping		VRAM B Mapping	
FB_A_EDC0	EDC0.A	FB_B_EDC0	EDC0.A
FB_A_EDC1	EDC0.B	FB_B_EDC1	EDC0.B
FB_A_EDC2	EDC0.C	FB_B_EDC2	EDC0.C
FB_A_EDC3	EDC0.D	FB_B_EDC3	EDC0.D
FB_A_EDC4	EDC0.E	FB_B_EDC4	EDC0.E
FB_A_EDC5	EDC0.F	FB_B_EDC5	EDC0.F
FB_A_EDC6	EDC0.G	FB_B_EDC6	EDC0.G
FB_A_EDC7	EDC0.H	FB_B_EDC7	EDC0.H
FB_A_EDC8	EDC0.I	FB_B_EDC8	EDC0.I
FB_A_EDC9	EDC0.J	FB_B_EDC9	EDC0.J
FB_A_EDC10	EDC0.K	FB_B_EDC10	EDC0.K
FB_A_EDC11	EDC0.L	FB_B_EDC11	EDC0.L
FB_A_EDC12	EDC0.M	FB_B_EDC12	EDC0.M
FB_A_EDC13	EDC0.N	FB_B_EDC13	EDC0.N
FB_A_EDC14	EDC0.O	FB_B_EDC14	EDC0.O
FB_A_EDC15	EDC0.P	FB_B_EDC15	EDC0.P
FB_A_EDC16	EDC0.Q	FB_B_EDC16	EDC0.Q
FB_A_EDC17	EDC0.R	FB_B_EDC17	EDC0.R
FB_A_EDC18	EDC0.S	FB_B_EDC18	EDC0.S
FB_A_EDC19	EDC0.T	FB_B_EDC19	EDC0.T
FB_A_EDC20	EDC0.U	FB_B_EDC20	EDC0.U
FB_A_EDC21	EDC0.V	FB_B_EDC21	EDC0.V
FB_A_EDC22	EDC0.W	FB_B_EDC22	EDC0.W
FB_A_EDC23	EDC0.X	FB_B_EDC23	EDC0.X
FB_A_EDC24	EDC0.Y	FB_B_EDC24	EDC0.Y
FB_A_EDC25	EDC0.Z	FB_B_EDC25	EDC0.Z



Close to GDDR6 UG11

Around GDDR6 UG11

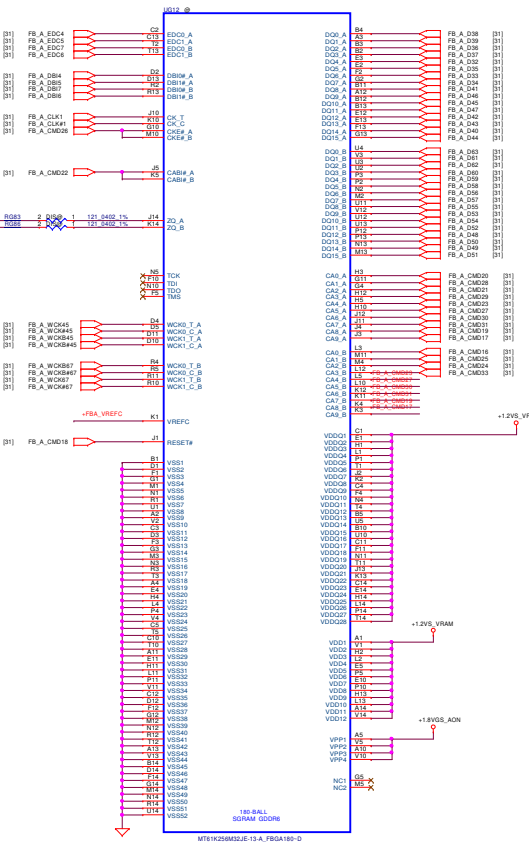


Close to GDDR6 UG11

Close to +1.8VGS_AON

Close to GDDR6 UG11

Close to +1.8VGS_AON



Close to GDDR6 UG12

Around GDDR6 UG12

Close to GDDR6 UG12

Close to +1.8VGS_AON

Close to GDDR6 UG12

Close to +1.8VGS_AON

Close to GDDR6 UG12

Close to +1.8VGS_AON

Close to GDDR6 UG12

Close to +1.8VGS_AON

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Close to +1.8VGS_AON

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Close to GDDR6 UG12

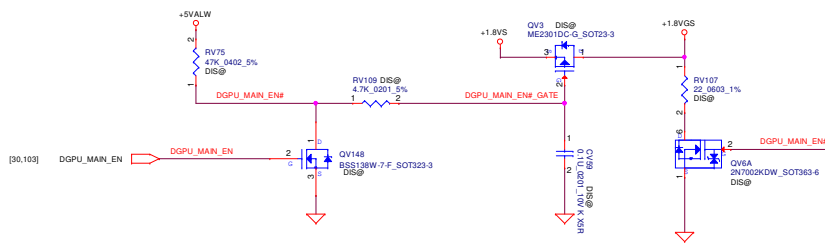
Close to +1.8VGS_AON

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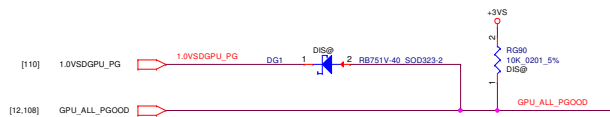
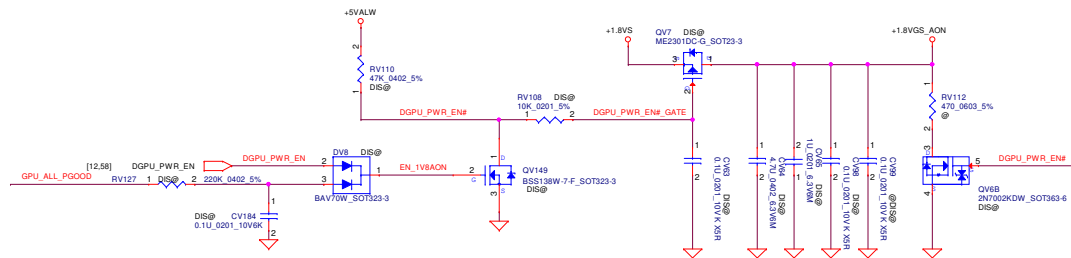
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+1.8VS to +1.8VGS



+1.8VS to +1.8VGS_AON



7.3.2.1 Power-Up Sequence

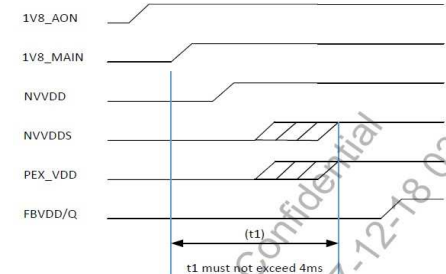
The following power-up sequence is required:

1V8_AON → 1V8_MAIN → NVVDD → NVVDDS / PEX_DVDD → FBVDD(Q)

► All GPU power rails must ramp up after 1V8_AON.

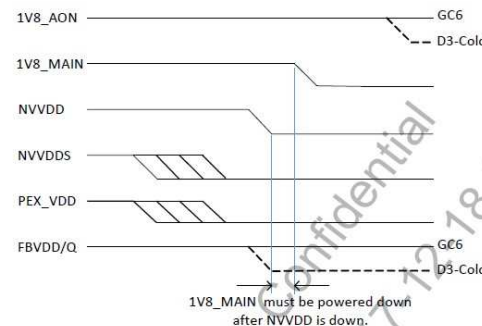
► FBVDD(Q) should ramp up after NVVDDS and PEX_DVDD.

All other 1.8V power rails can ramp up with 1V8_MAIN including PEX_HVDD and all PLLVDD rails; all other 1V power rails can ramp up with PEX_DVDD.



re 7.5 Example of Power-Up Sequencing Order

7.3.2.2 Power-Down Sequence



1V8_MAIN must be powered down after NVVDD is down.

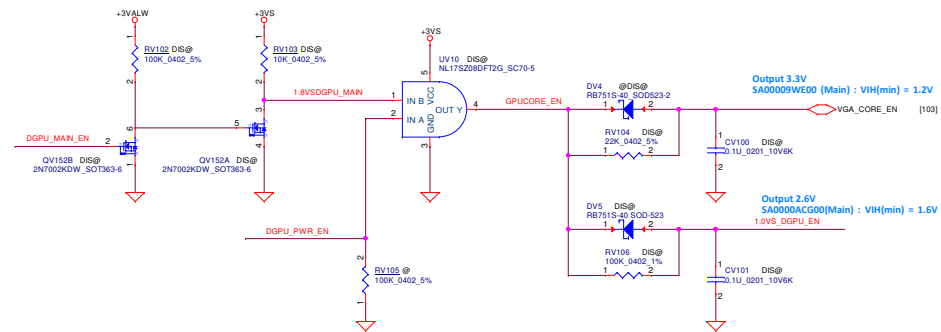
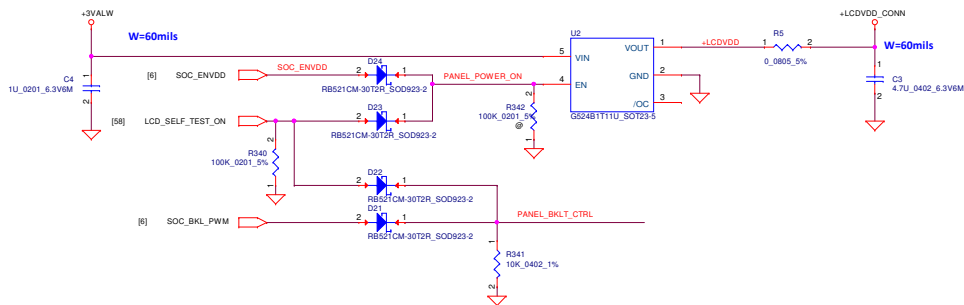


Figure 8.9 GC OFF Entry/Exit Timing Diagram

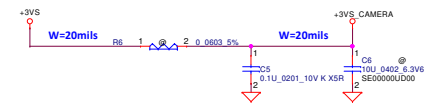
Table 8.1 GC OFF Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

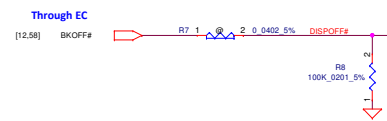
LCD POWER SWITCH



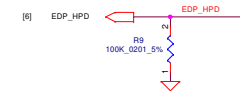
CAMERA POWER CIRCUIT



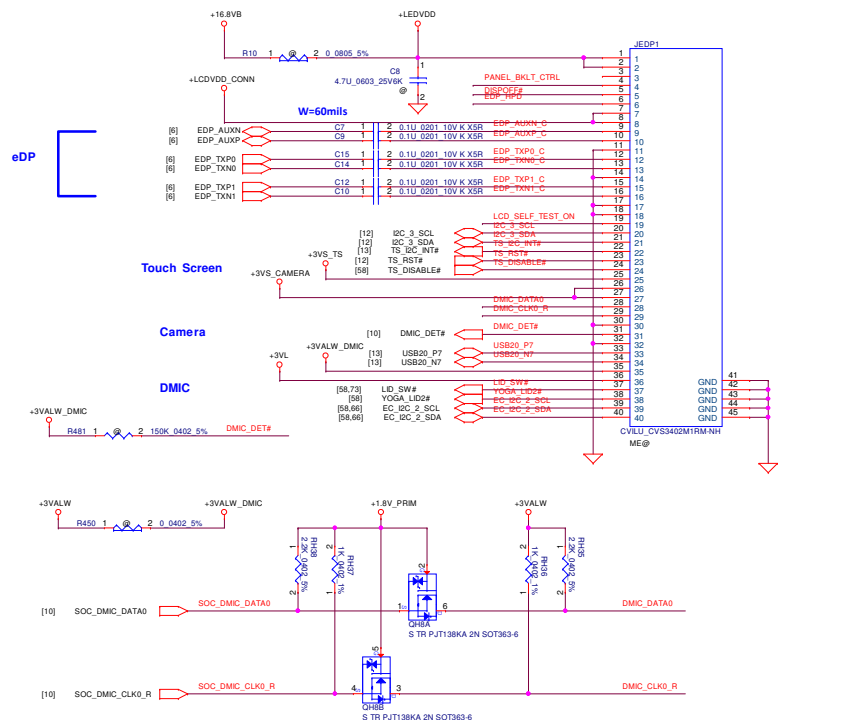
DISPLAY OFF



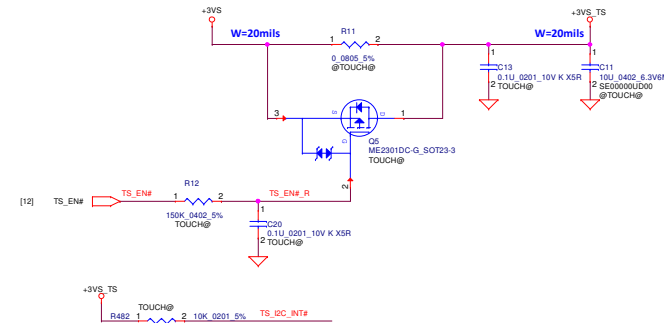
HOT PLUG DETECT



eDP CONNECTOR

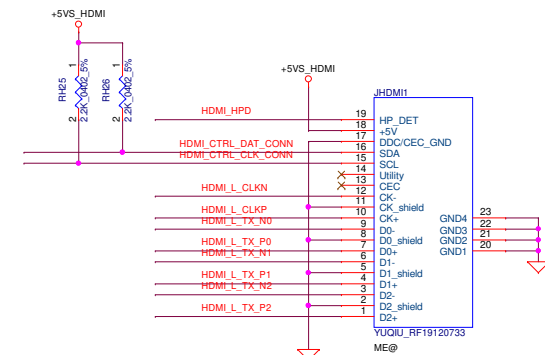
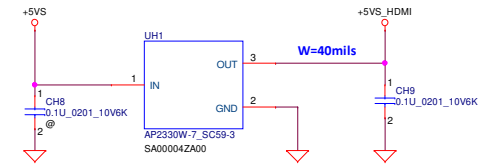
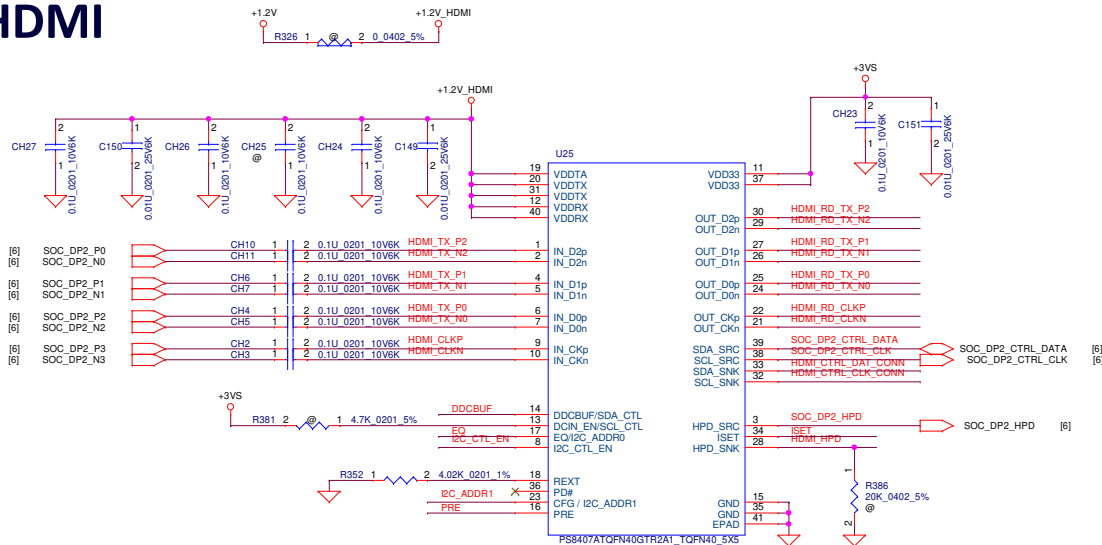


Touch Screen POWER CIRCUIT

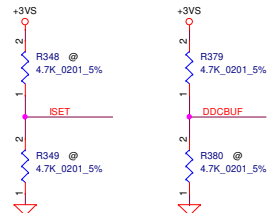


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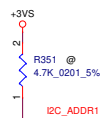
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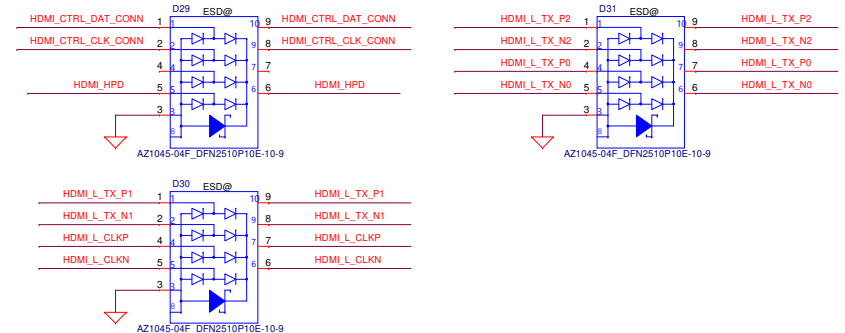
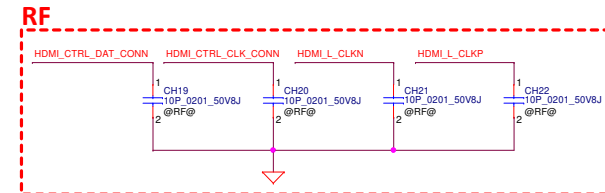
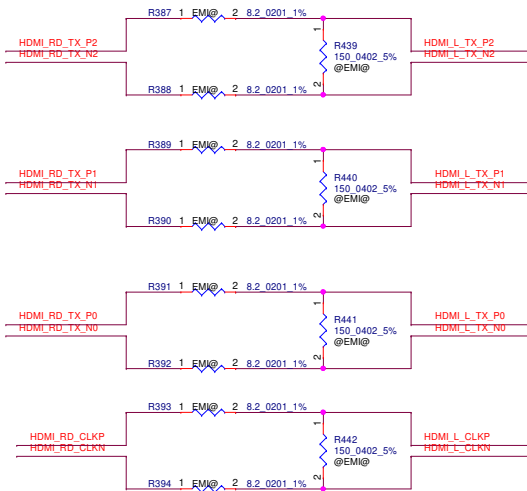
```
Output pre-emphasis setting; Internal pull down at ~150kohm, 3.3V I/O.
L: no pre-emphasis
H: 1.6dB pre-emphasis
M: 2.5dB pre-emphasis
```



```
TMS output swing adjustment; Internal pull down at ~150kohm, 3.3V I/O.
L: default
M: increase +13%
M: reduce -13%
```



```
I2C control bus address LSB; Internal pull down at ~150kohm, 3.3V I/O.
[I2C_ADDR1, I2C_ADDR0]=
  LL: 0x4C/4D (default)
  LH: 0x5C/5D
  HL: 0xCC/CD
  HH: 0xEC/ED
```



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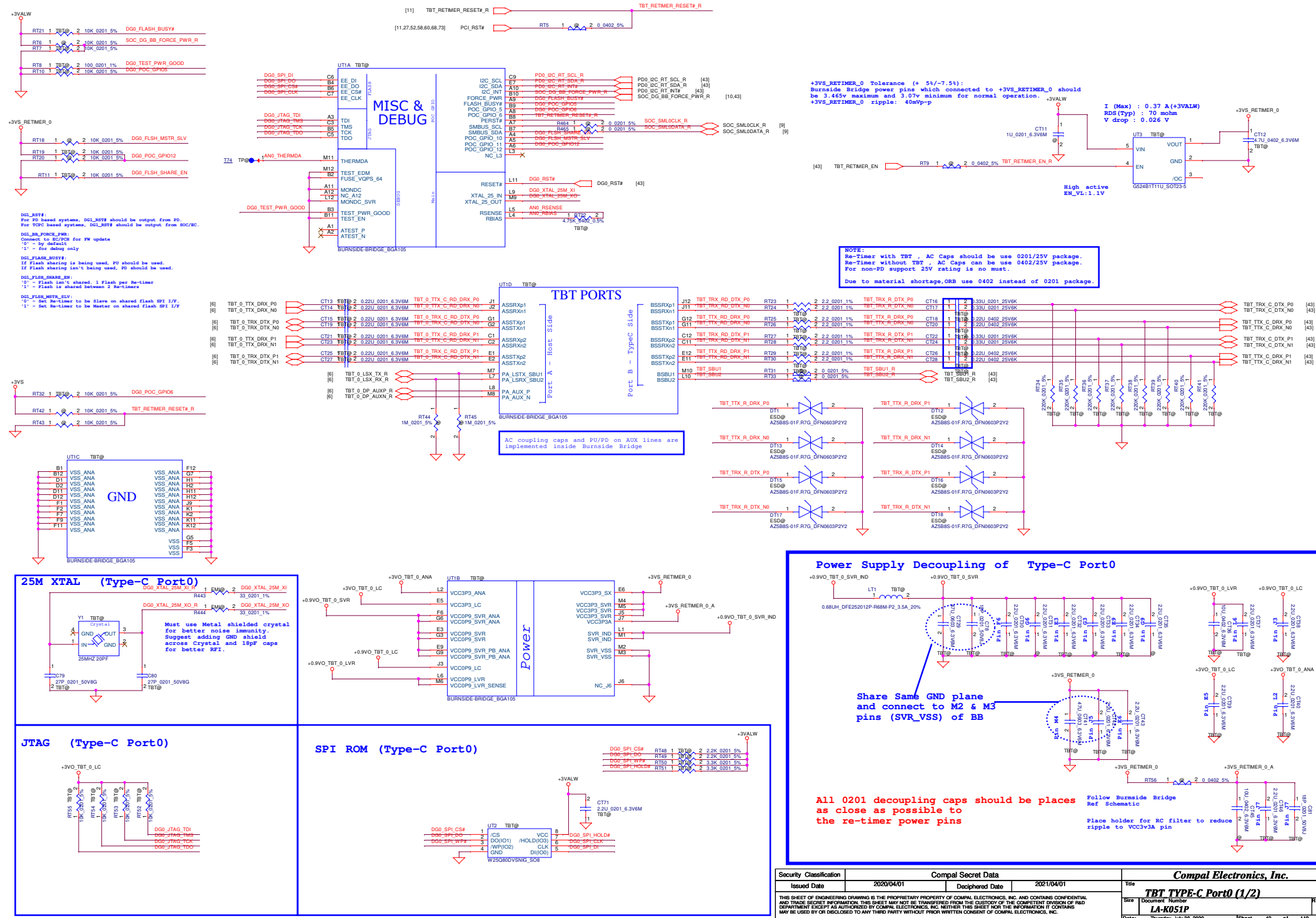
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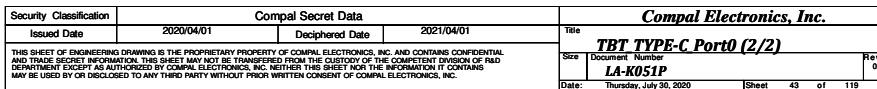
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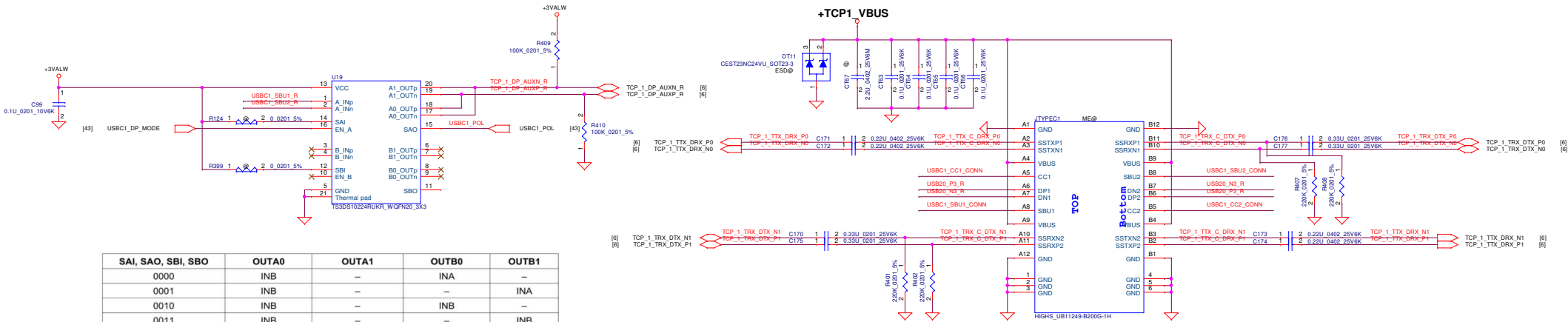
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MB USB3.1 TypeC Conn. (Port 0/ Re-Timer Master)

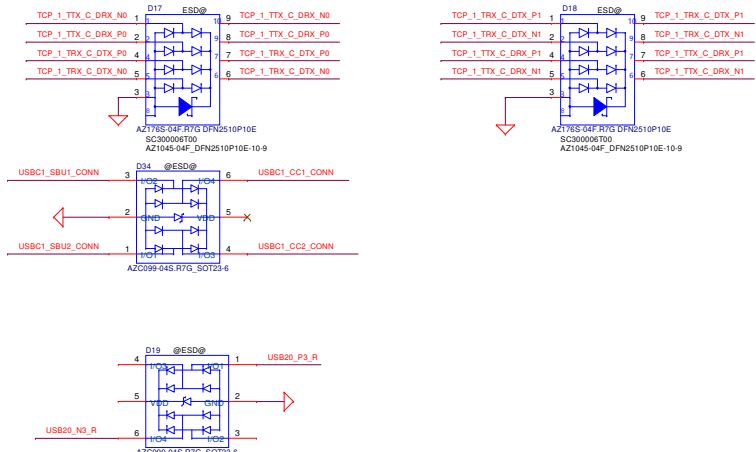
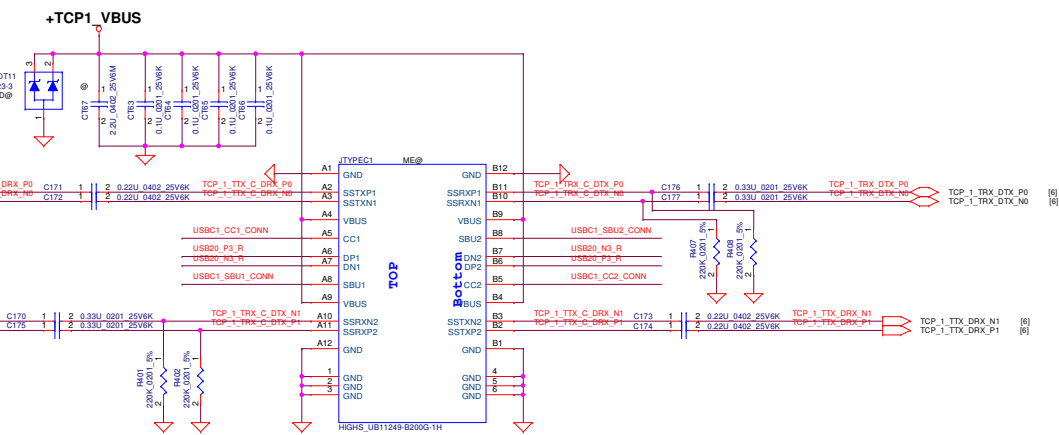
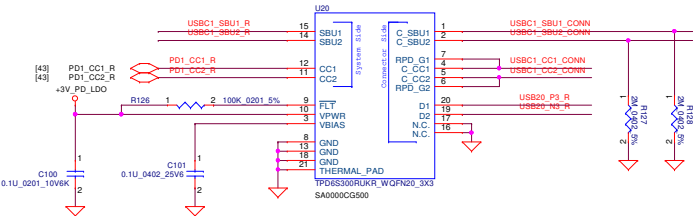




Type-C PORT 1



SAI, SAO, SBI, SBO	OUTA0	OUTA1	OUTB0	OUTB1
0000	INB	—	INA	—
0001	INB	—	—	INA
0010	INB	—	INB	—
0011	INB	—	—	INB
0100	—	INB	INA	—
0101	—	INB	—	INA
0110	—	INB	INB	—
0111	—	INB	—	INB
1000	INA	—	INA	—
1001	INA	—	—	INA
1010	INA	—	INB	—
1011	INA	—	—	INB
1100	—	INA	INA	—
1101	—	INA	—	INA
1110	—	INA	INB	—
1111	—	INA	—	INB



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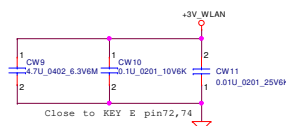
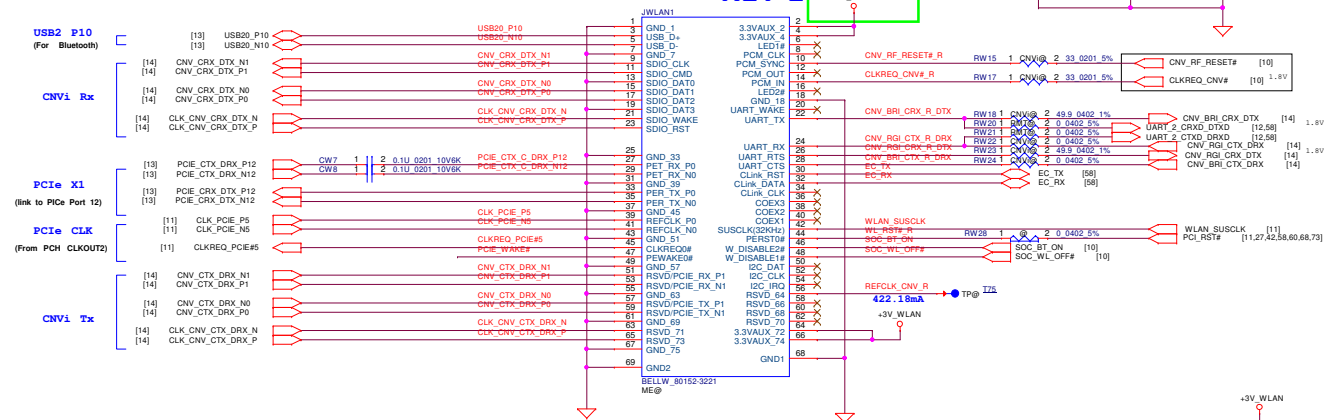
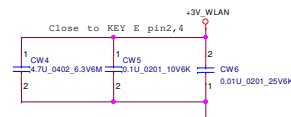
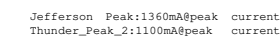
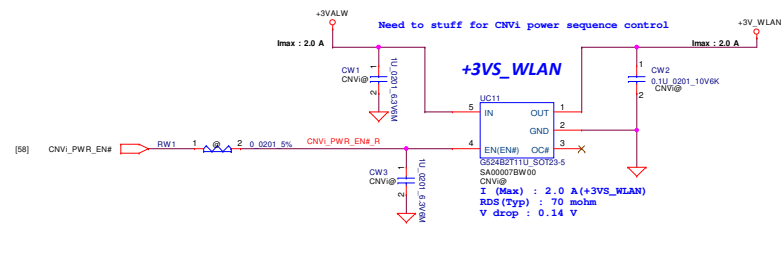
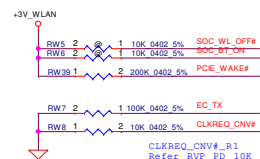
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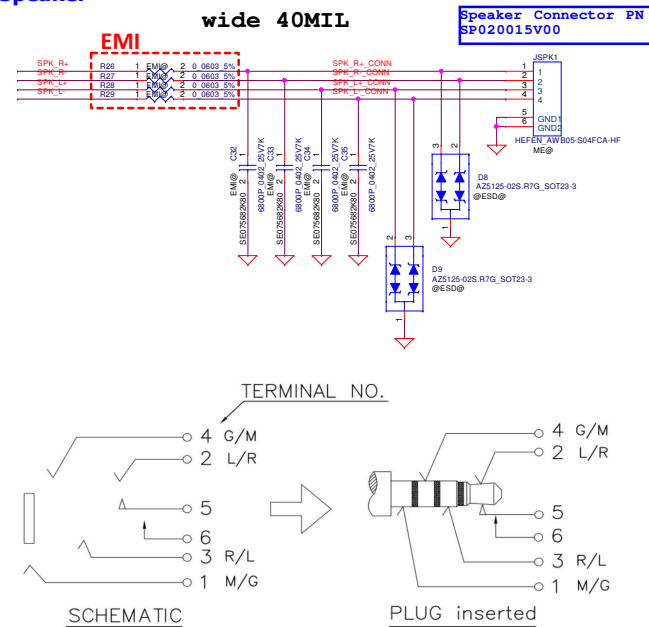
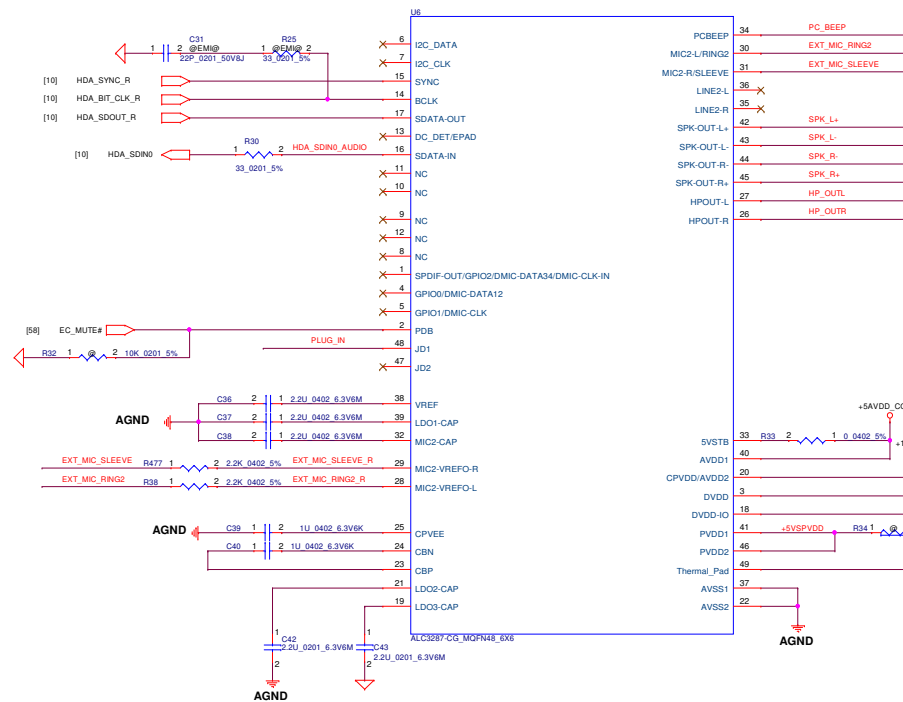
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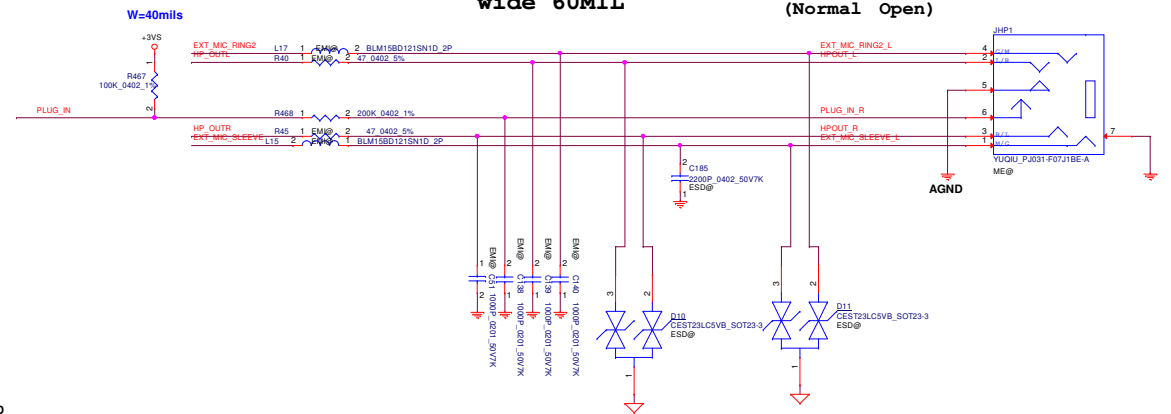
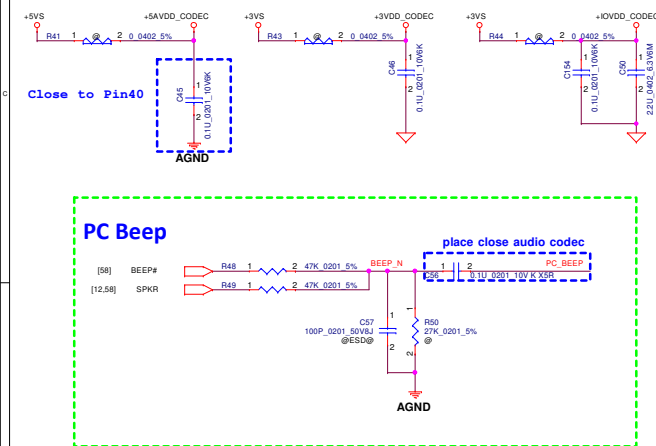
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Speaker

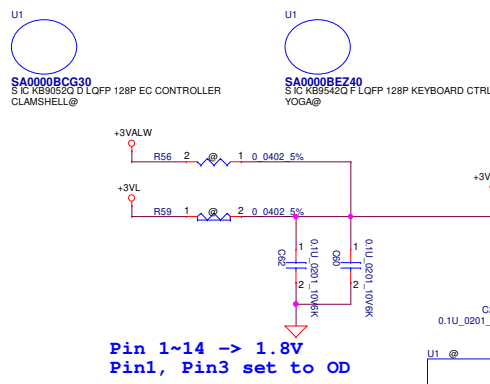
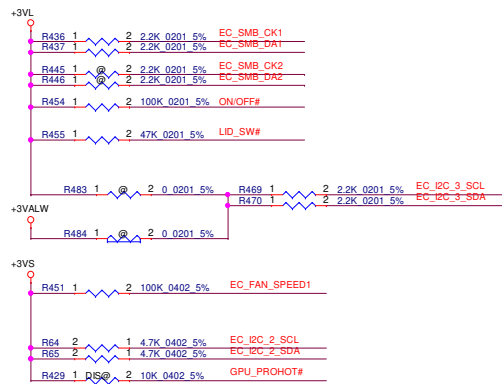


For vendor suggest
+5AVDD_CODEC use VS power

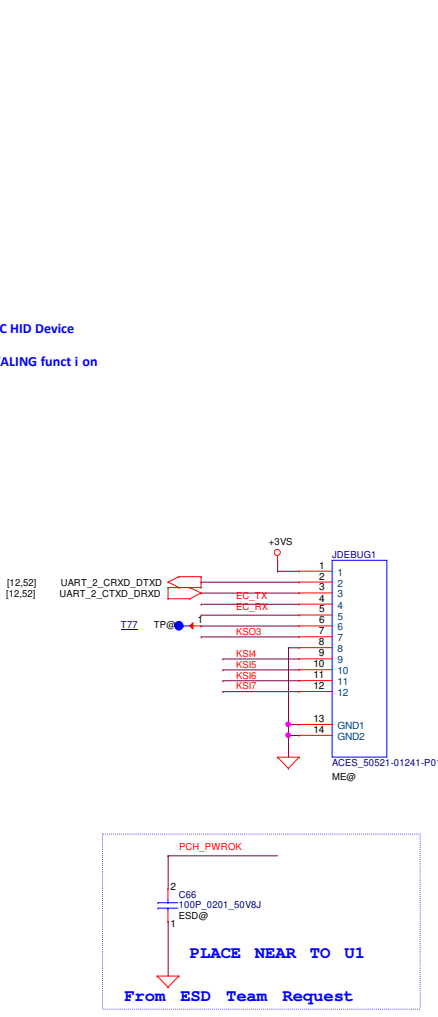
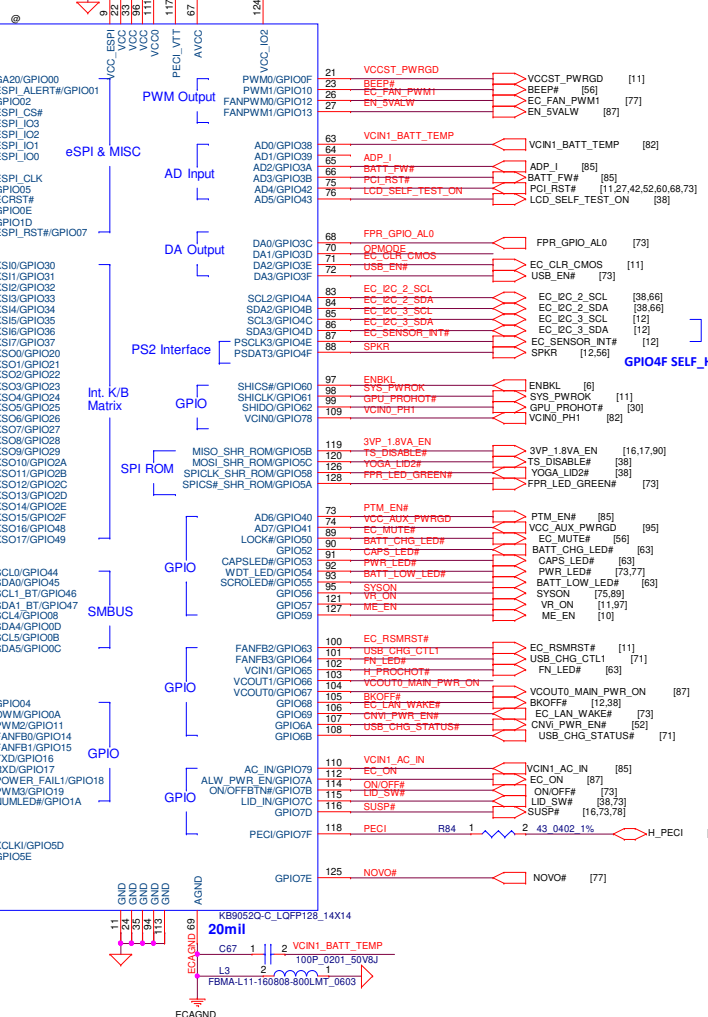
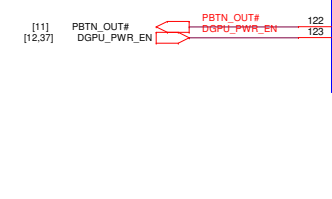
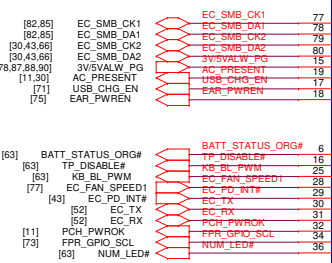
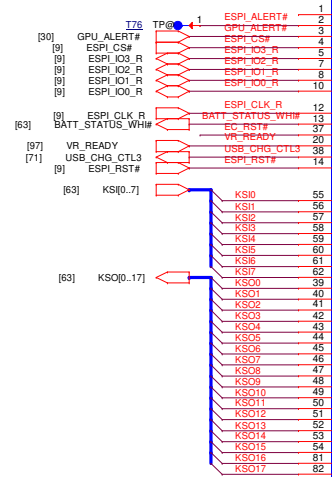
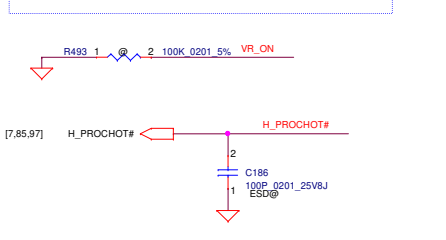
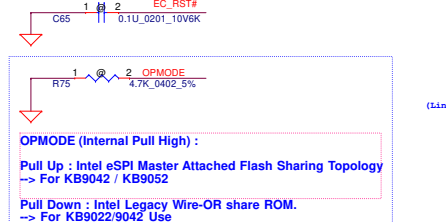
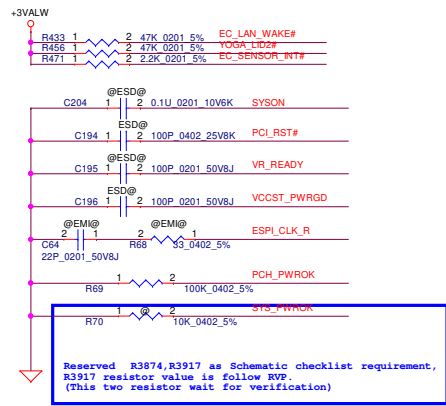


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Pin 1~14 -> 1.8V
Pin1, Pin3 set to OD



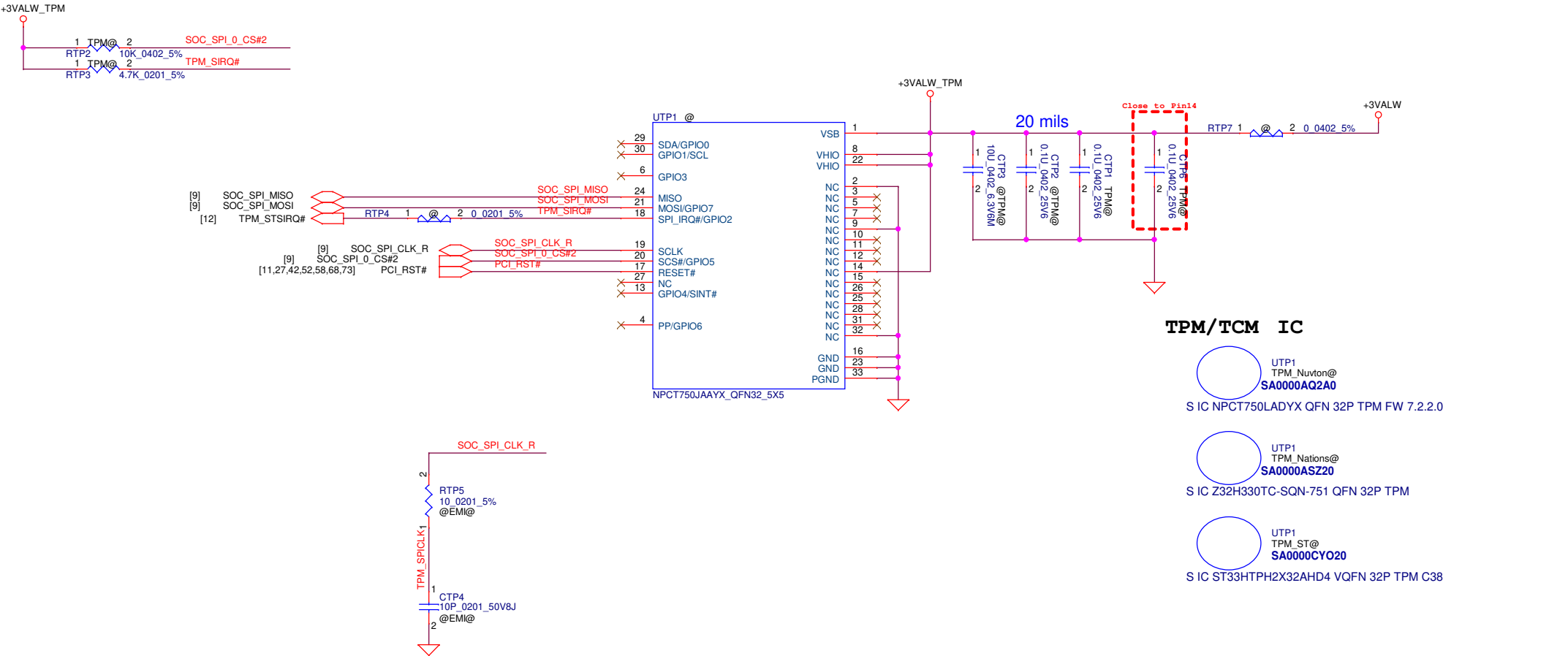
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TPM 2.0 Co-lay

- 1.Nuvton_NPCT750LABYX
2.ST_ST33HTPH2E32AAE8
3.Nations_Z32H330TC



- TPM/TCM IC**
- UTP1
TPM_Nuvton@
SA0000AQ2A0
S IC NPCT750LADYX QFN 32P TPM FW 7.2.2.0
 - UTP1
TPM_Nations@
SA0000ASZ20
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 - UTP1
TPM_ST@
SA0000CYO20
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Size		Document Number		Rev	
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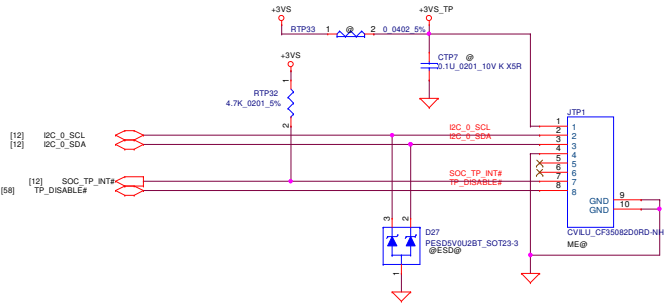
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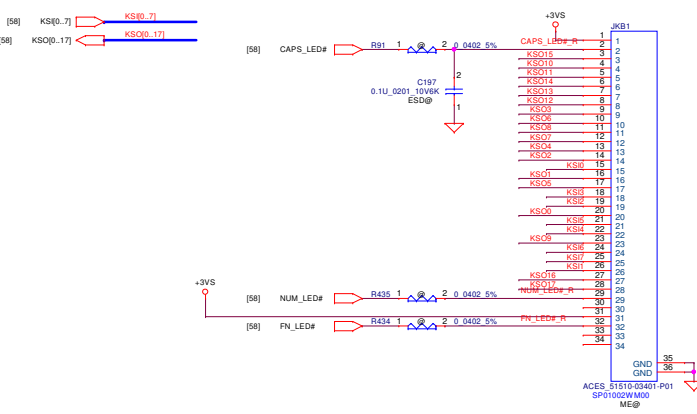
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				Size	Document Number
				LA-K051P	
Date: Thursday, July 30, 2020				Sheet	62 of 119
				Rev	0.3

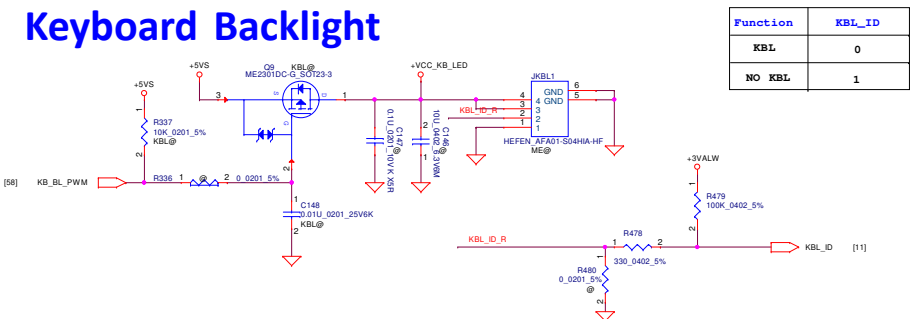
Touch Pad



Keyboard

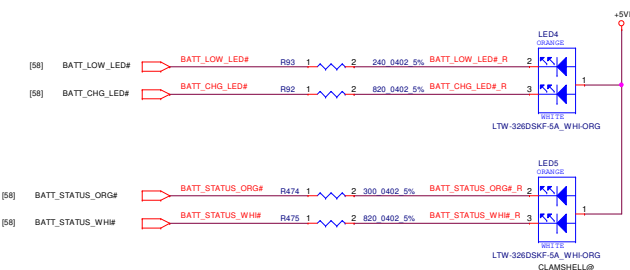


Keyboard Backlight



Function	KBL_ID
KBL	0
NO KBL	1

BATT LED



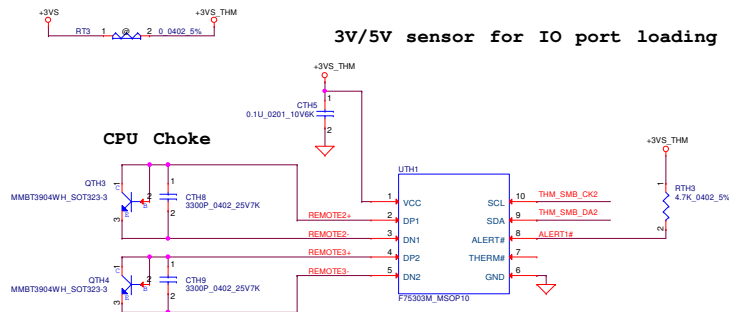
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				Size	Document Number
				LA-K051P	
Date: Thursday, July 30, 2020				Sheet	64 of 119
				Rev	0.3

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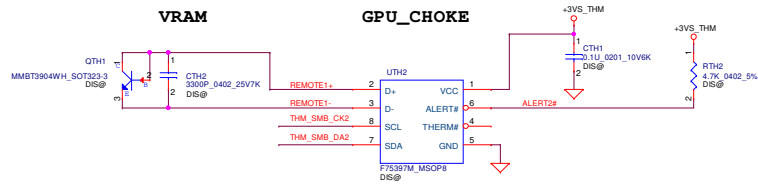
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				Size	Document Number
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Date: Thursday, July 30, 2020				Sheet	65 of 119
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Thermal sensor

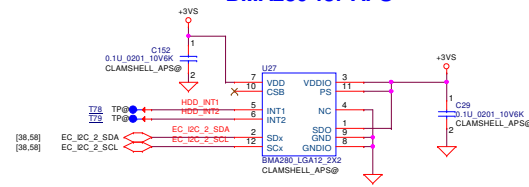


REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length<8"

Charger CHOKE

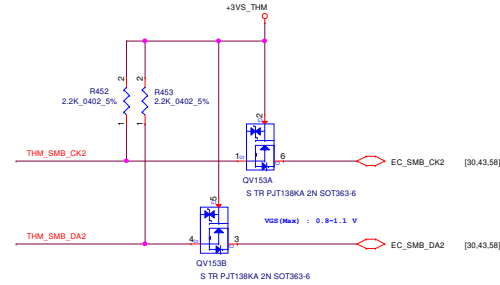


BMA280 for APS



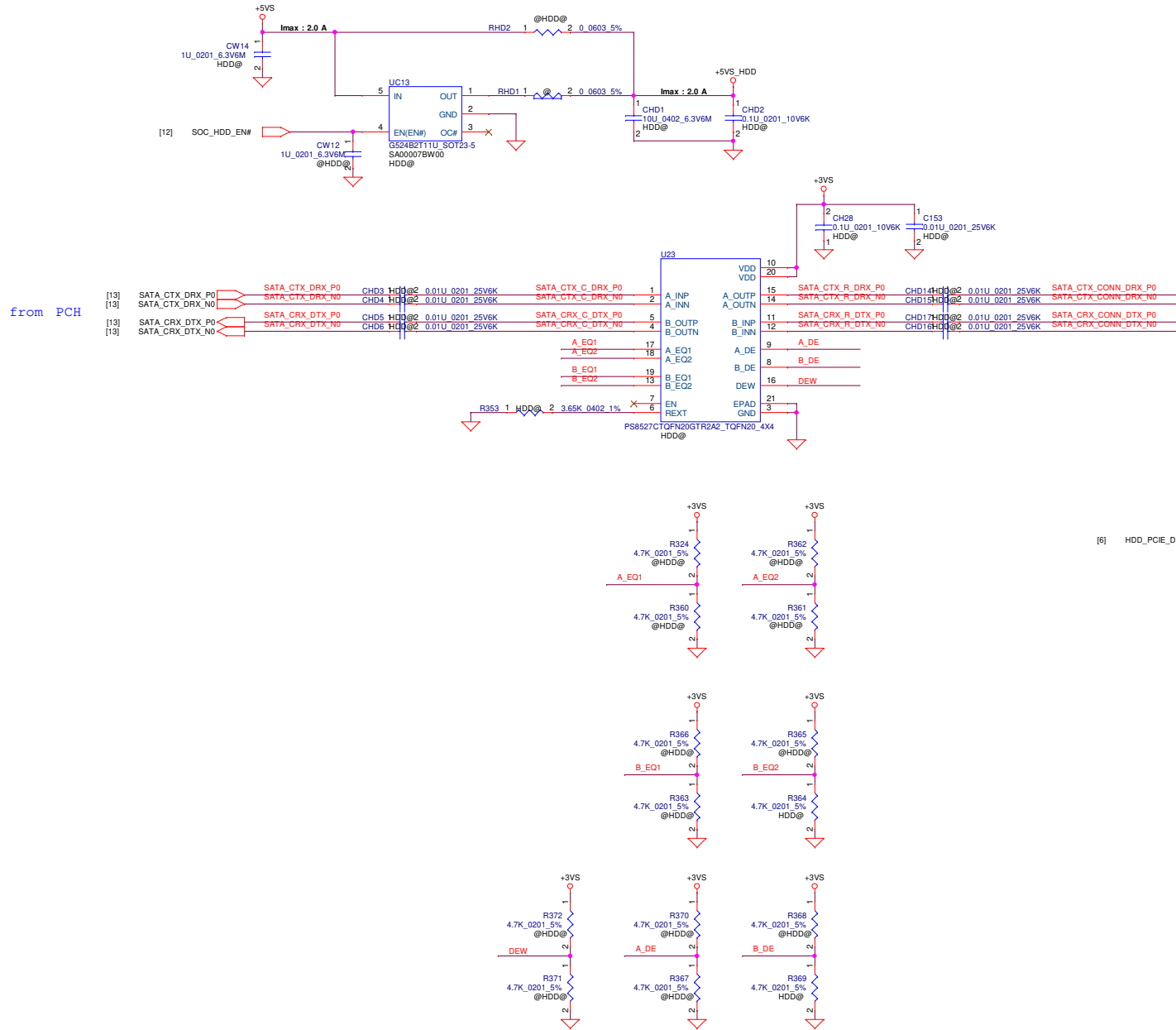
I2C Address: 0x19

BMA253 for YOGA G-Sensor

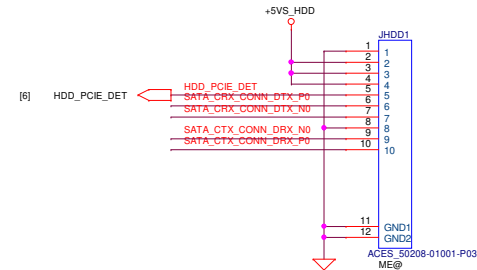


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				Document Number	LA-K051P
				Date	Thursday, July 30, 2020
				Sheet	66 of 119

SATA HDD

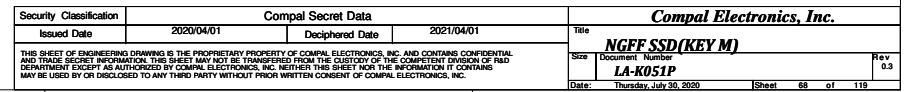


SATA HDD Conn.



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SSD PCIE



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				Size	Rev
				Document Number	0.3
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				Date:	Thursday, July 30, 2020
				Sheet	70 of 119

[illegible]

2A/Active Low

W=80mils

W=80mils

USB_CHG_EN

USB_OC#

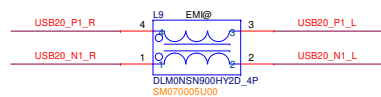
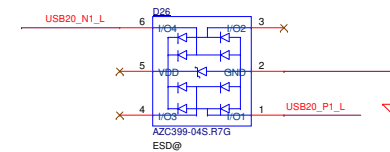
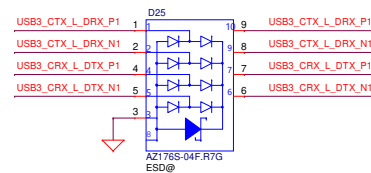
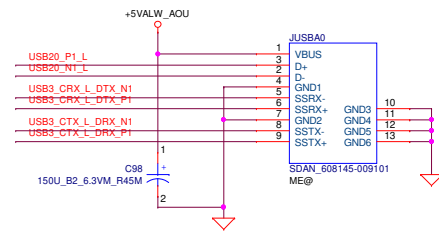
USB_OC#

USB20_N1

USB20_P1

USB20_N1_R

USB20_P1_R

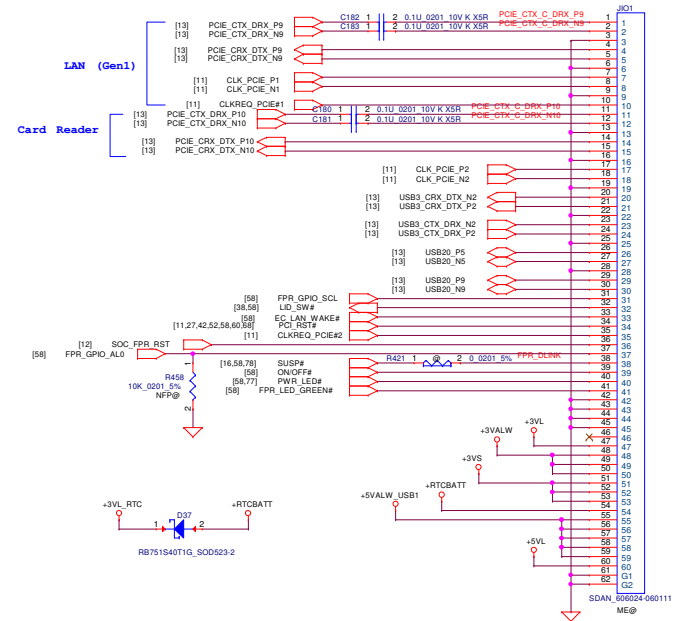
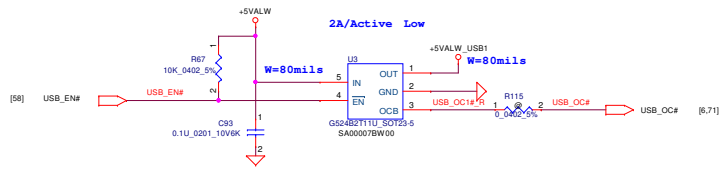


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				Sheet	72 of 119
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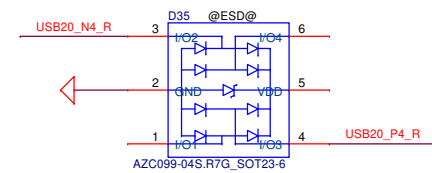
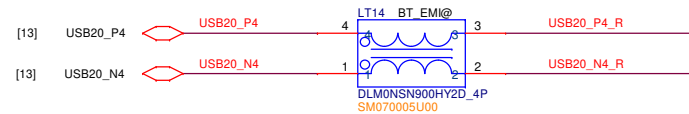
USB3.0_Port1 SW



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				Size	Document Number
				LA-K051P	
Date: Thursday, July 30, 2020				Sheet	74 of 119
				Rev	0.3

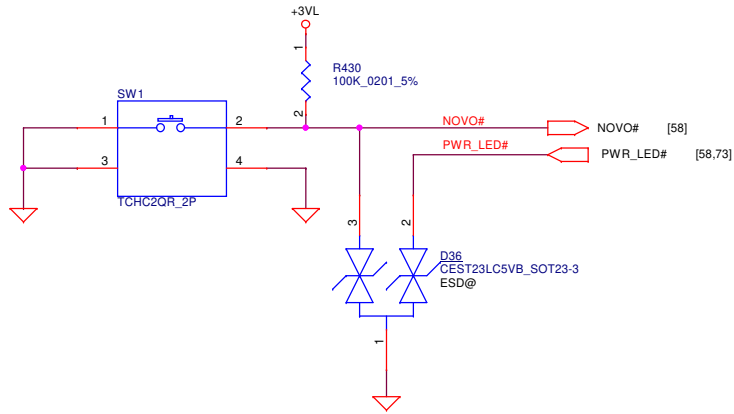


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				LA-K051P	
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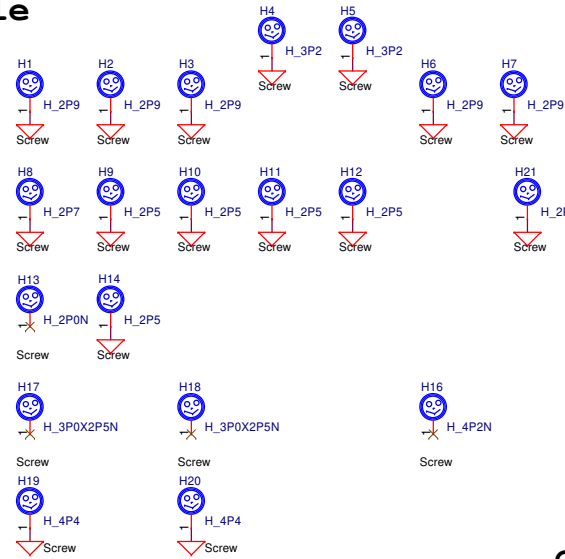
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				Size	Document Number
				LA-K051P	
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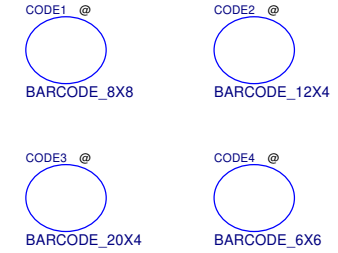
NOVO Button



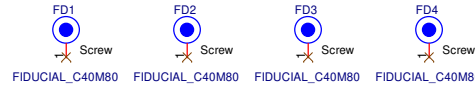
Screw Hole



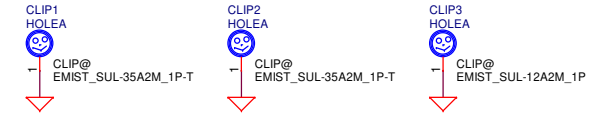
LASER BARCODE



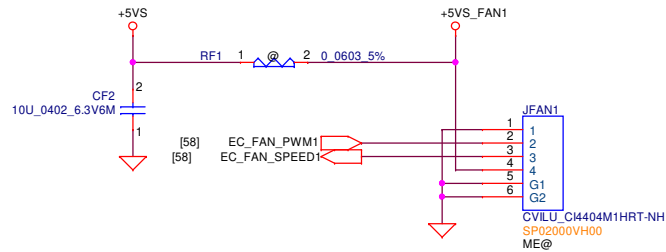
Fiducial Mark



Clip



CPU Fan Control Circuit



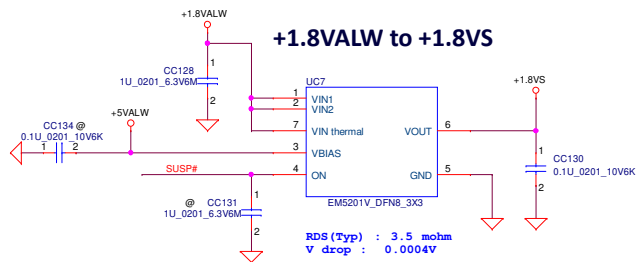
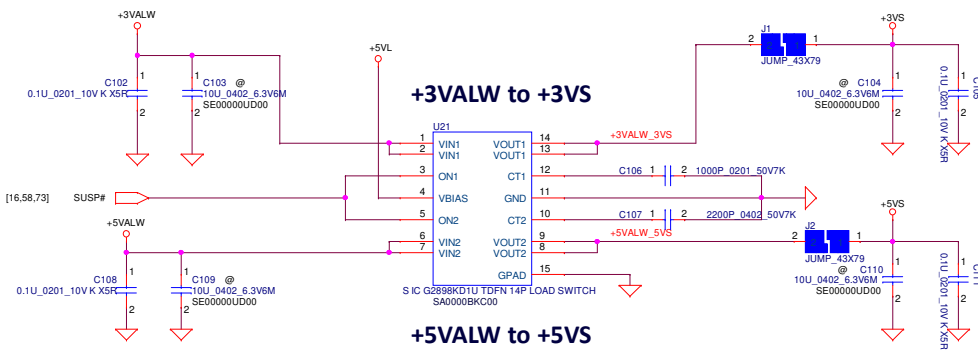
ZZZ
ALT. GROUP PARTS DRAM 8G SAM GLV3Y
X7688138LA4
DDR_S8G@

ZZZ
SMT EMC YOGA FOR EE AK051 GLV3Y
X4EAN738L51
ESD@

ZZZ
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X7688138LA1
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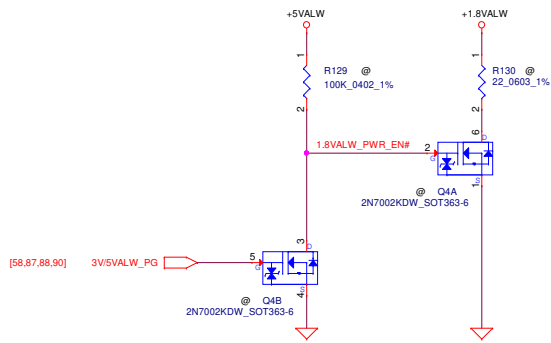
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DC to DC



DISCHARGE CIRCUIT

For +1.8VALW Discharge



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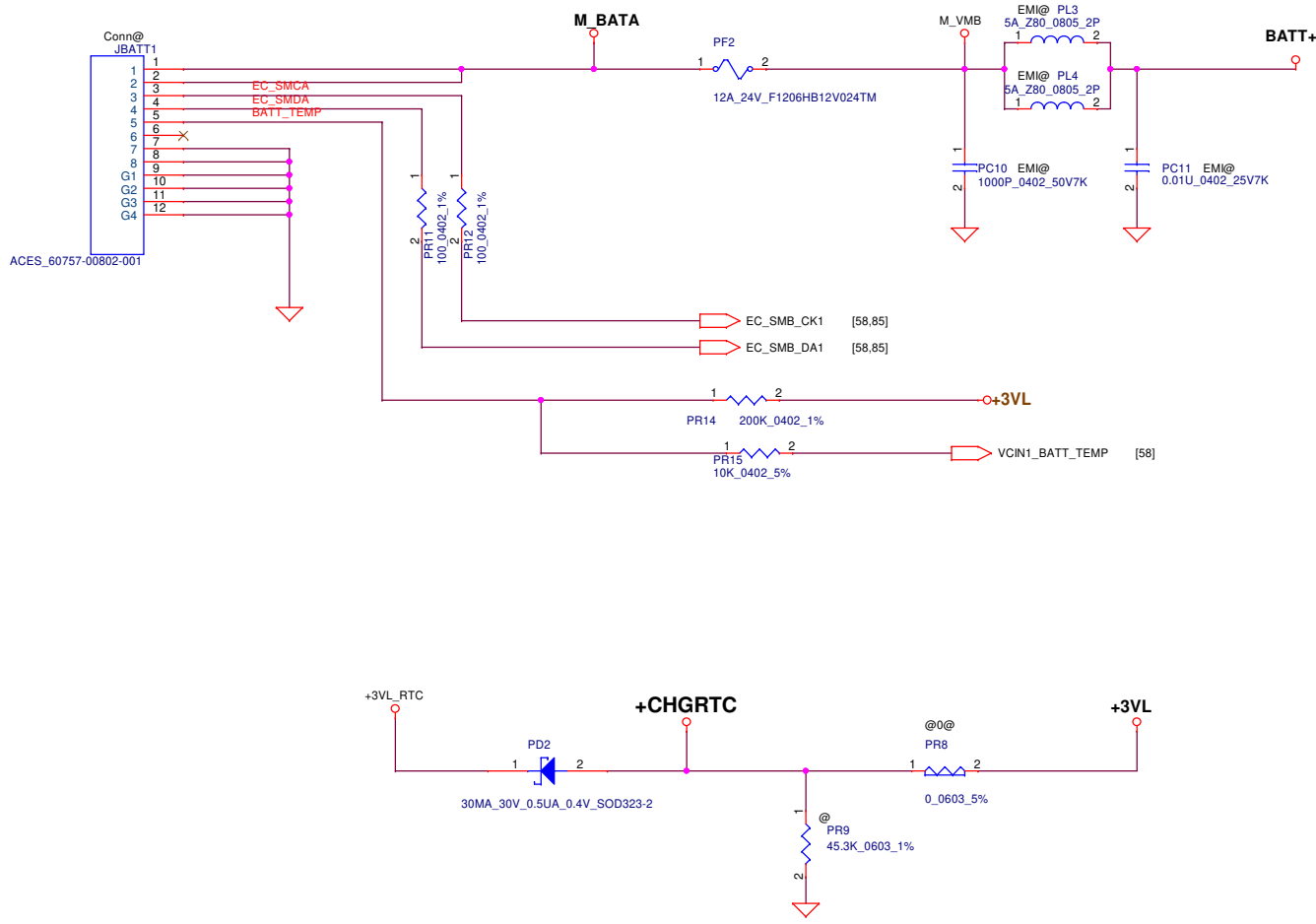
Security Classification	Compal Secret Data			Title	
Issued Date	2020/04/01	Deciphered Date	2021/04/01	XDP/CMC/APS Debug Conn	
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				Date:	Thursday, July 30, 2020
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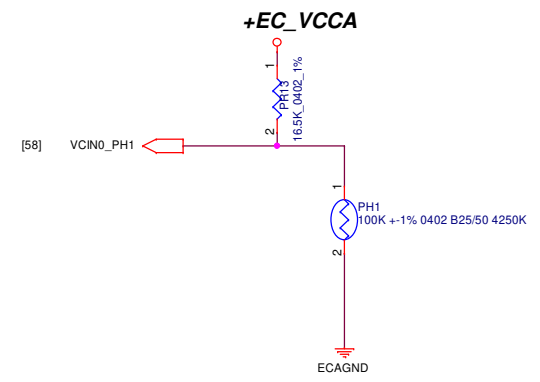
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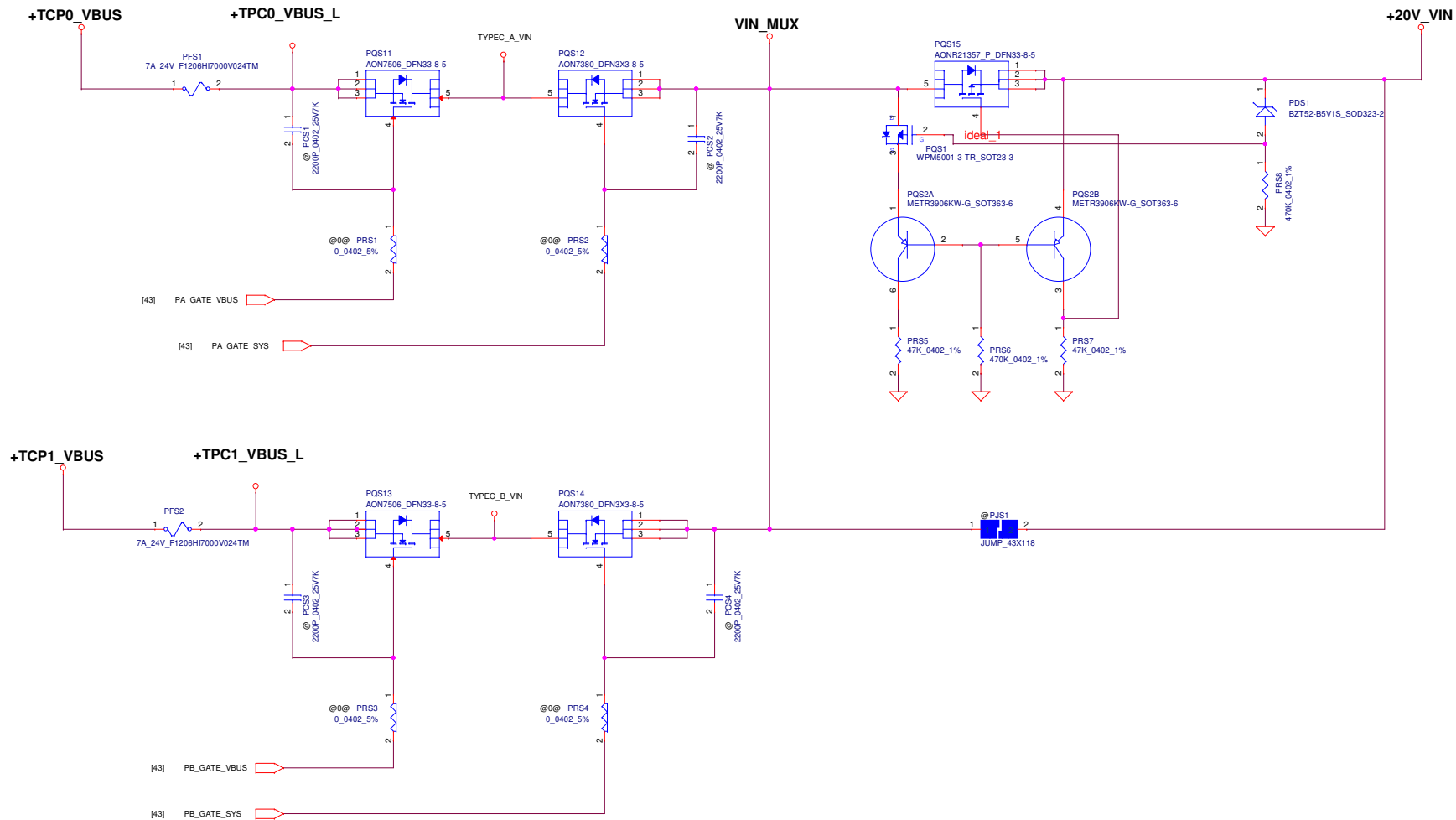
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				Size	Document Number	Rev
				Custom	LA-K051P	1.0
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PH201 under CPU bottom side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



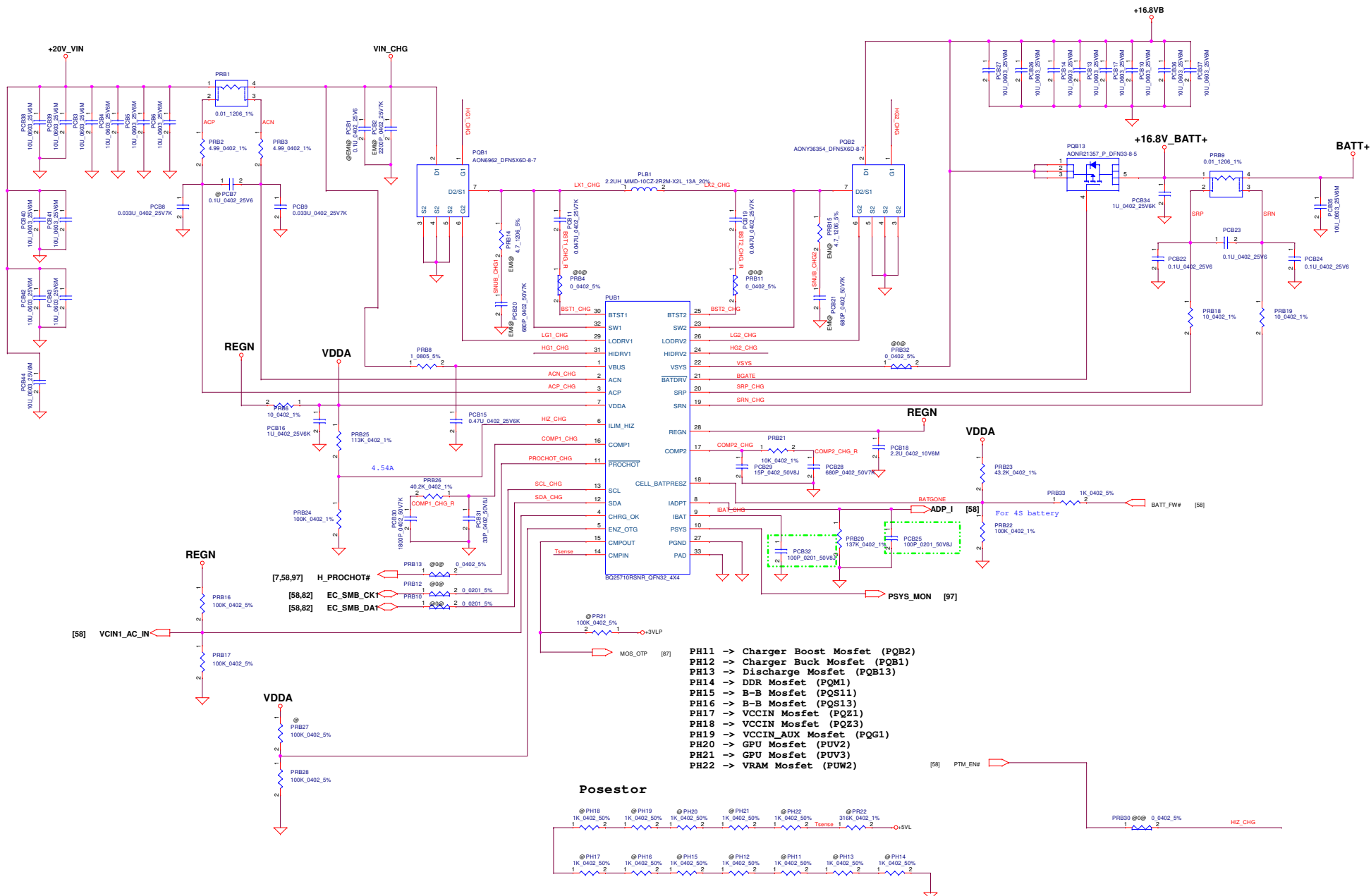
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				LA-K051P	
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Issued Date	2020/03/16	Deciphered Date	2020/12/09	Title	PWR- DC Conn/Type-C PD in
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				Rev	1.0
				Date:	Thursday, July 30, 2020
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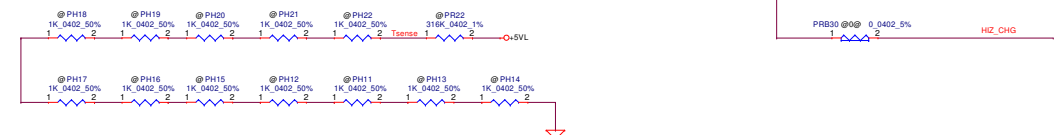
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				Size	Document Number	Rev
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- PH11 -> Charger Boost Mosfet (PQB2)
PH12 -> Charger Buck Mosfet (PQB1)
PH13 -> Discharge Mosfet (PQB13)
PH14 -> DDR Mosfet (PQM1)
PH15 -> B-B Mosfet (PQS11)
PH16 -> B-B Mosfet (PQS13)
PH17 -> VCCIN Mosfet (PQZ1)
PH18 -> VCCIN Mosfet (PQZ3)
PH19 -> VCCIN_AUX Mosfet (PQG1)
PH20 -> GPU Mosfet (PUV2)
PH21 -> GPU Mosfet (PUV3)
PH22 -> VRAM Mosfet (PUW2)

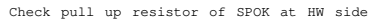
Posesor



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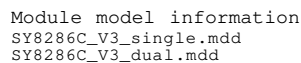
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SY8286B_V3_dual.mdd

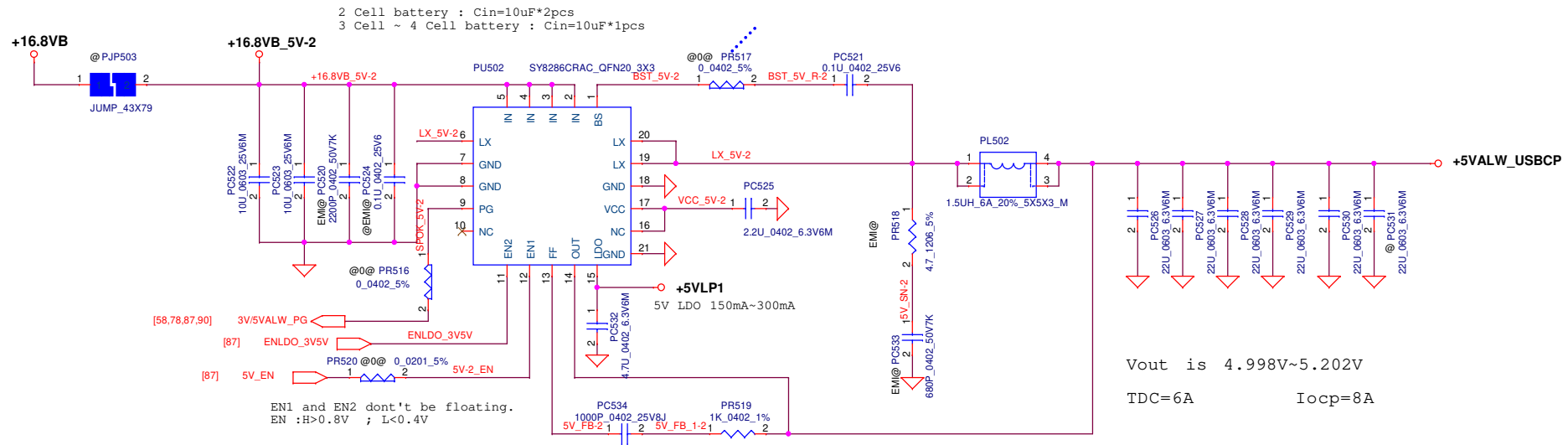


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Fsw : 600K Hz
EN1 and EN2 dont't be floating.
EN :H>1V ; L<0.4V
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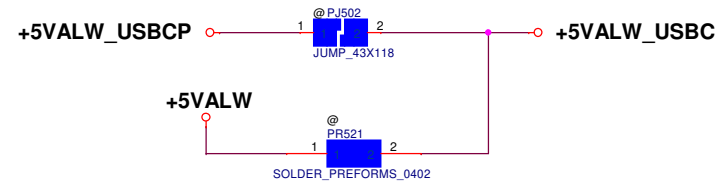
Vout is 3.234V~3.366V
TDC=6A Iocp=8A



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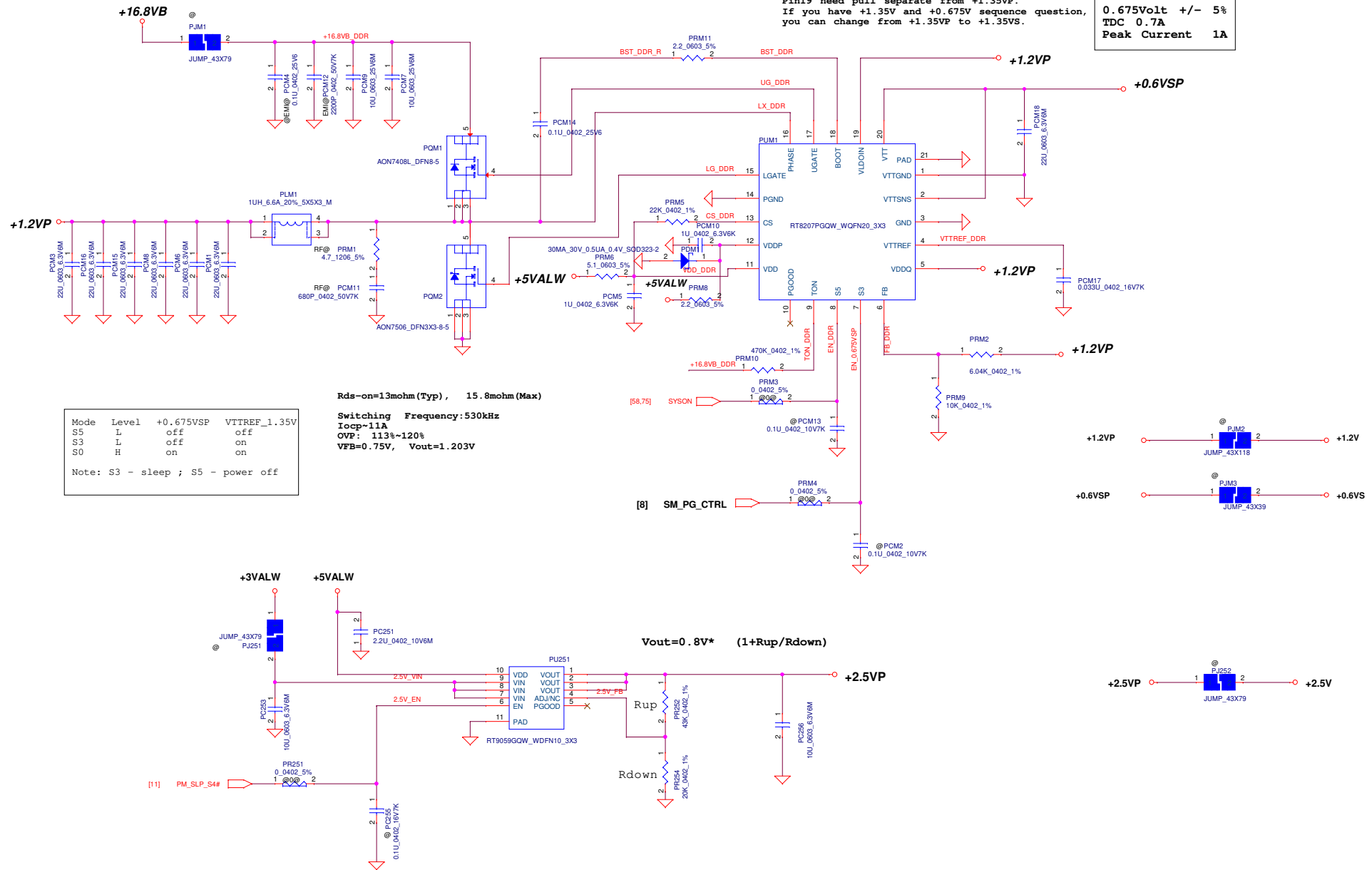
The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high.

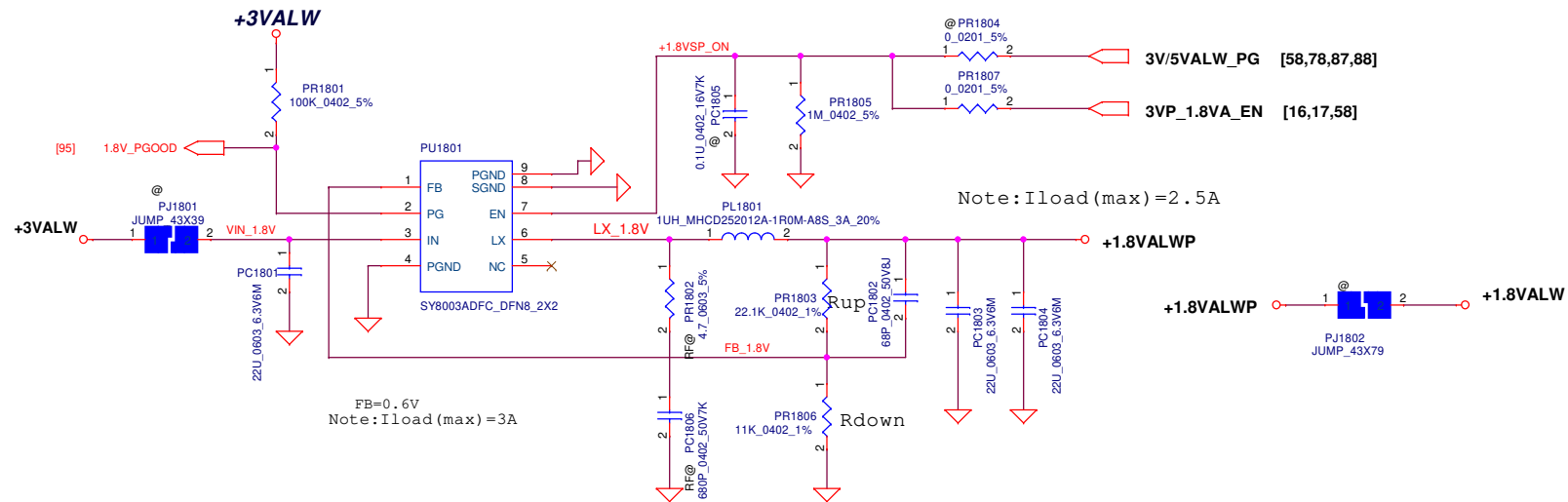


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Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A





Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

$$V_{out}=0.6V* (1+R_{up}/R_{down})$$

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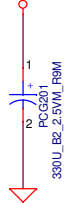
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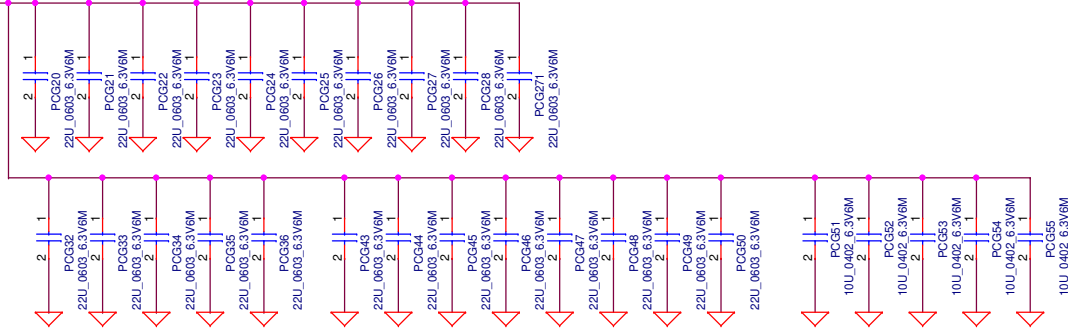
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+VCCIN_AUX

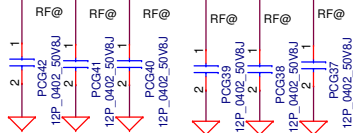


330U_R9
22U_0603 *1
*15

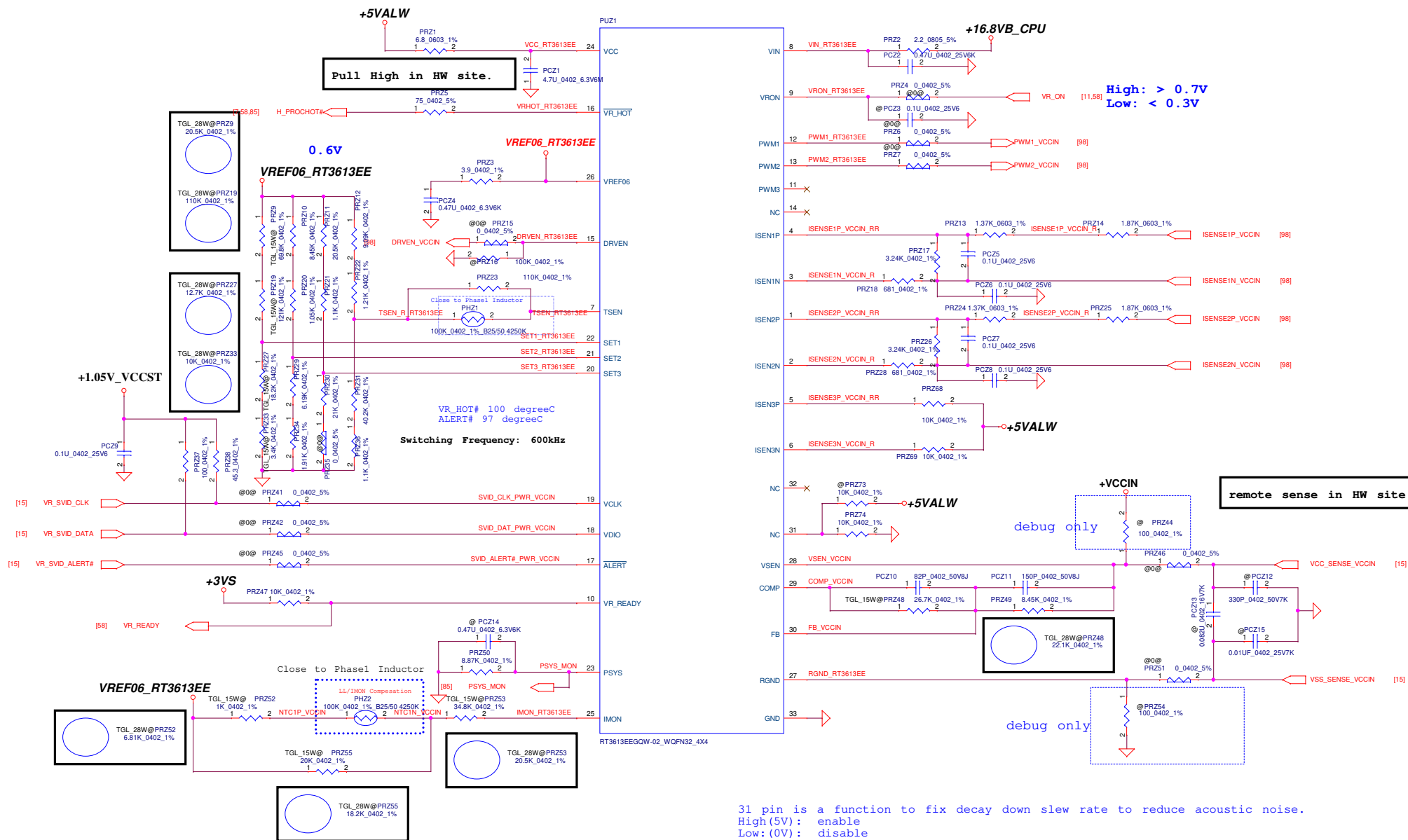
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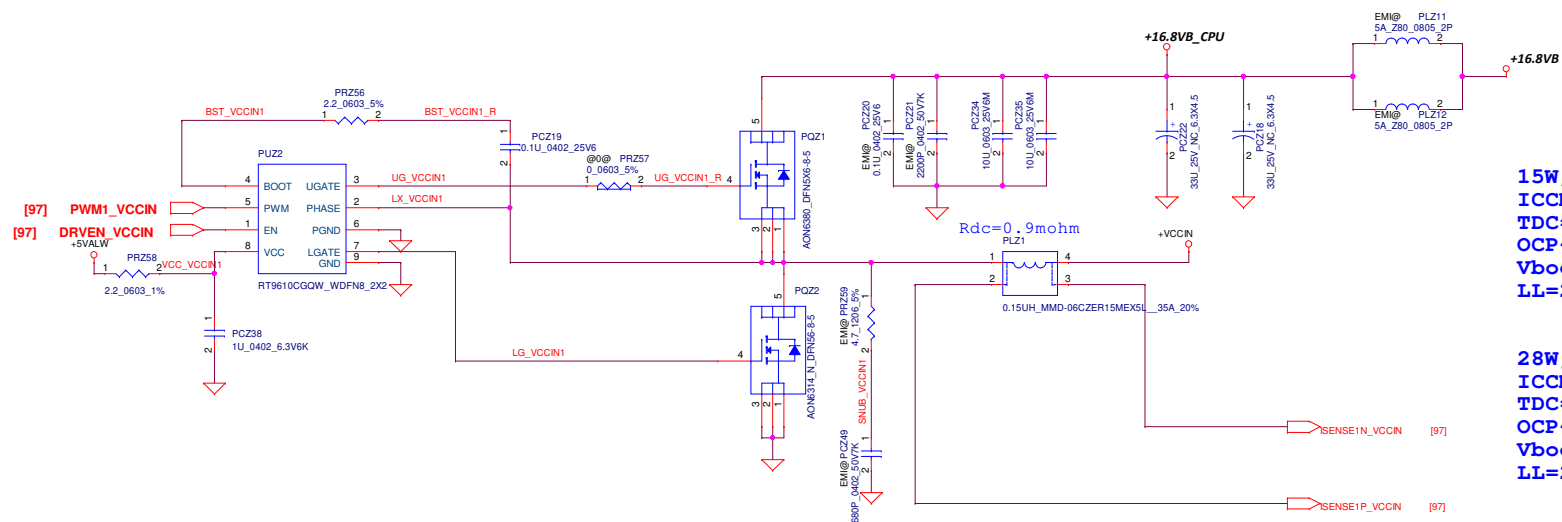
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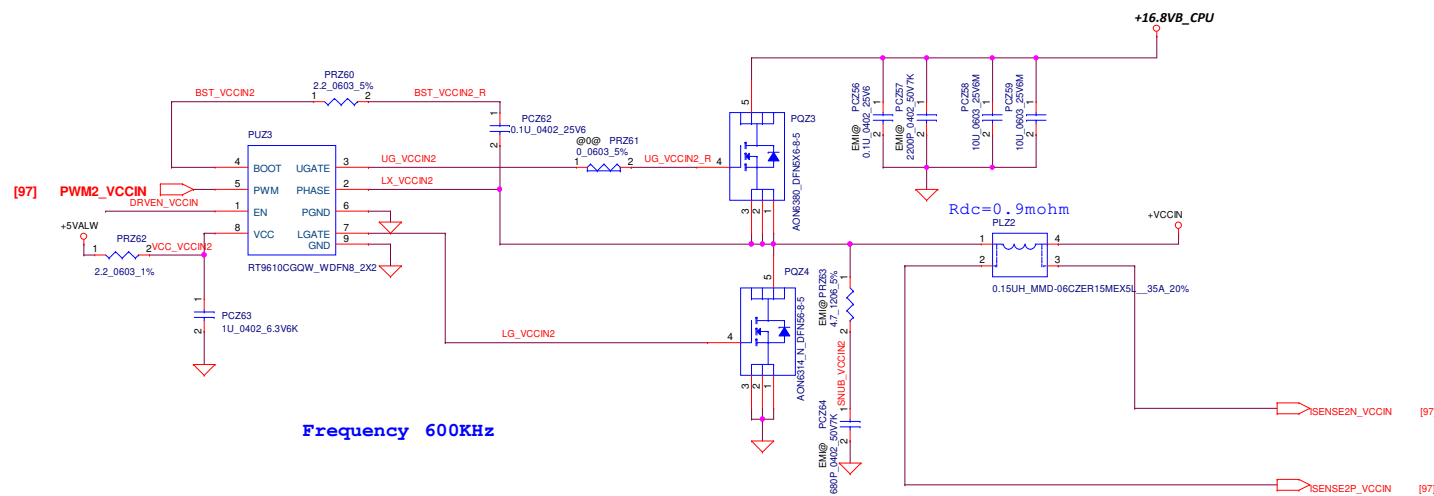


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15W, baseline:
ICCMAX=47A
TDC=30A
OCP~61.1A
Vboot=1.8V
LL=2mohm

28W, baseline:
ICCMAX=55A
TDC=36A
OCP~71.5A
Vboot=1.8V
LL=2mohm



Frequency 600KHz

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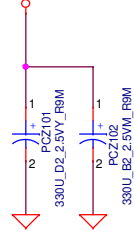
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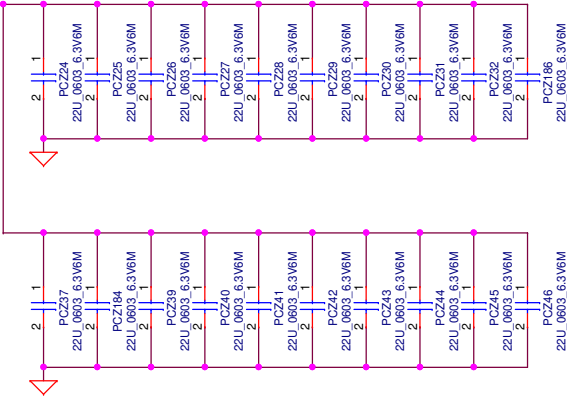
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+VCCIN

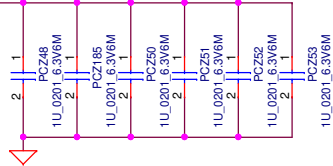


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22U_0603 *18
1U_0201 *6

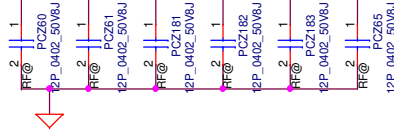
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+VCCIN



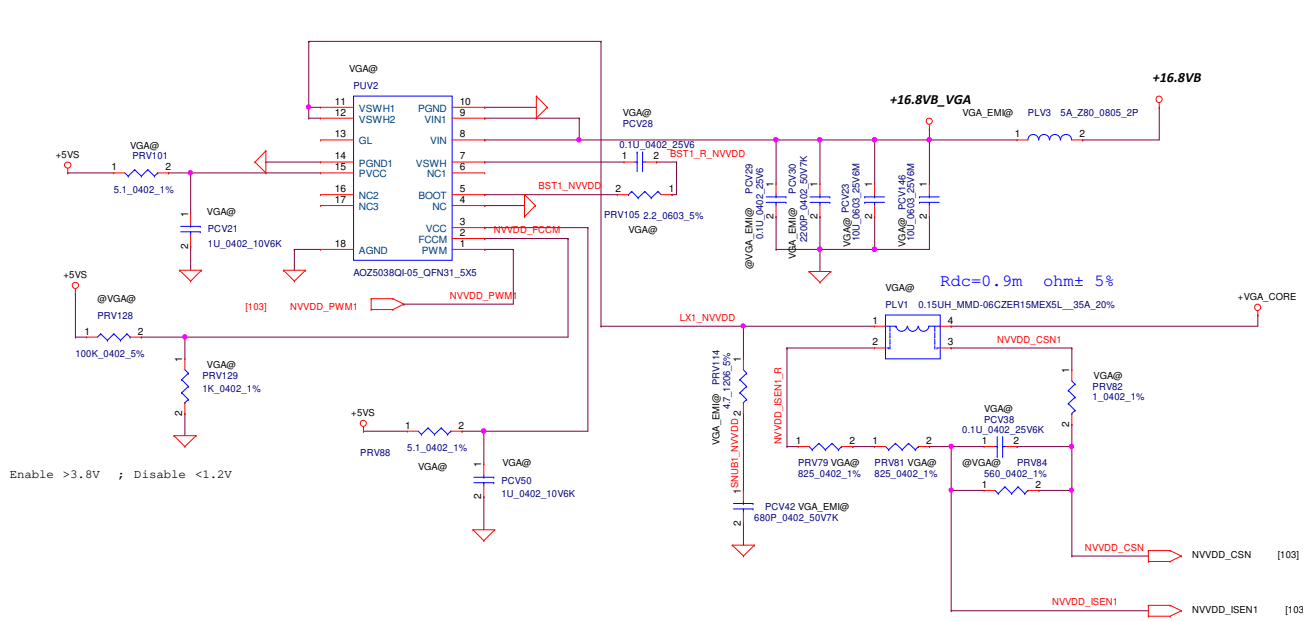
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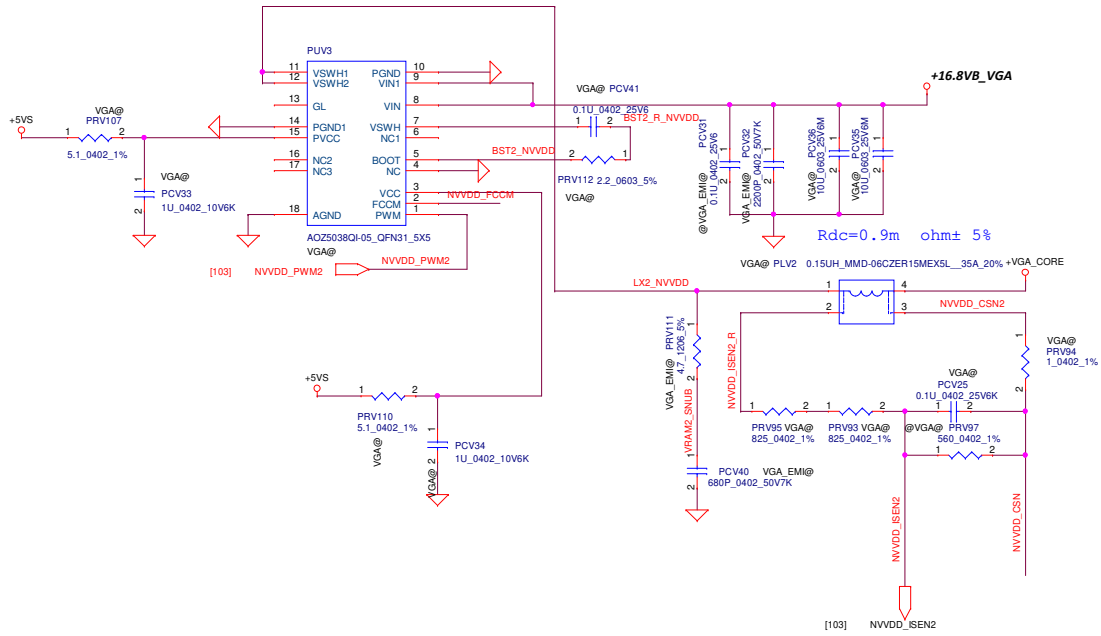
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+VGA CORE
EDP-Continuous 35A
EDP-Peak 75A
OCP > Need larger than (A)
Please base on GPU spec to calculate.

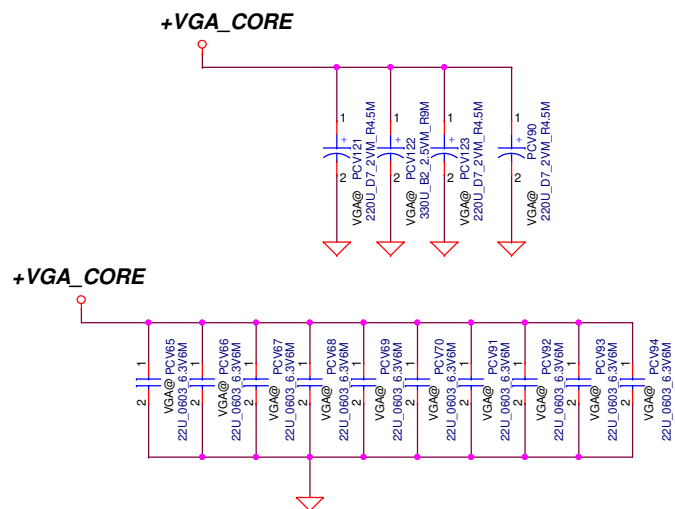


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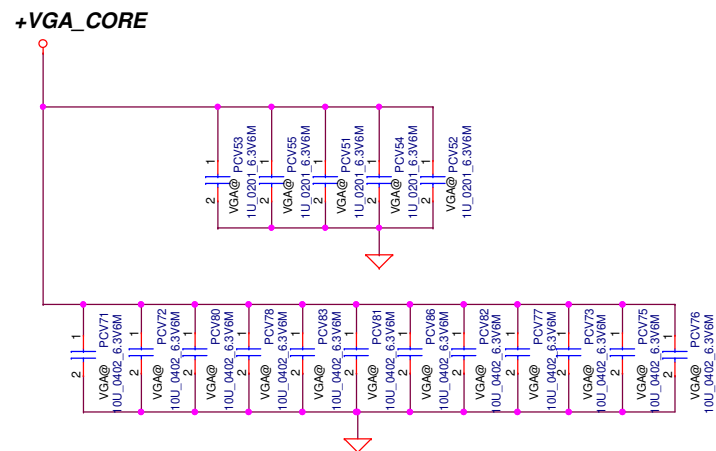
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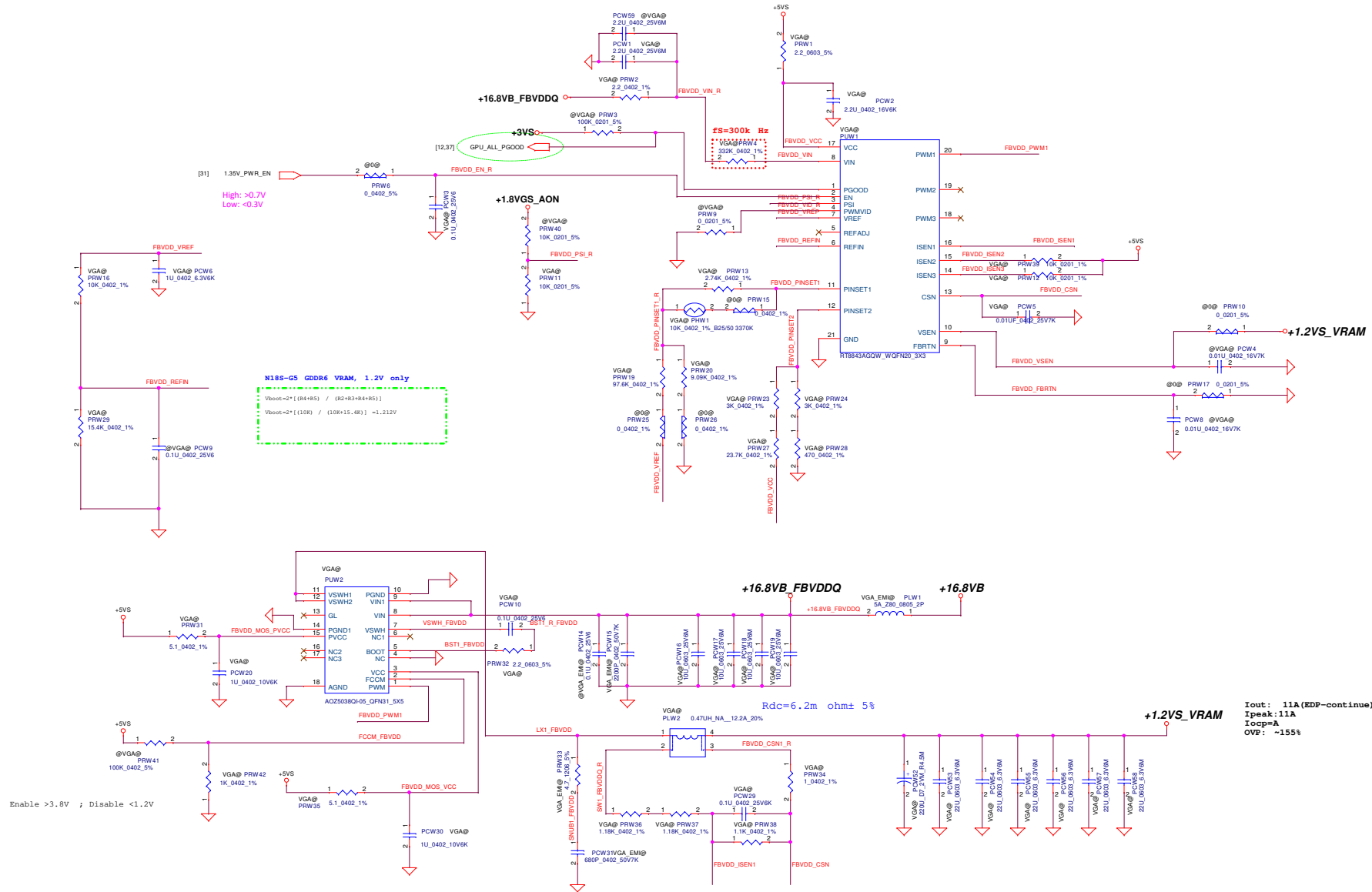
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VGA_CORE output cap
330U_B2_2.5V 1pcs
220U_D7_2.5V 3pcs
22U_0603_6.3V 10pcs
10U_0603_6.3V 12pcs
1U_0402_16V 5pcs

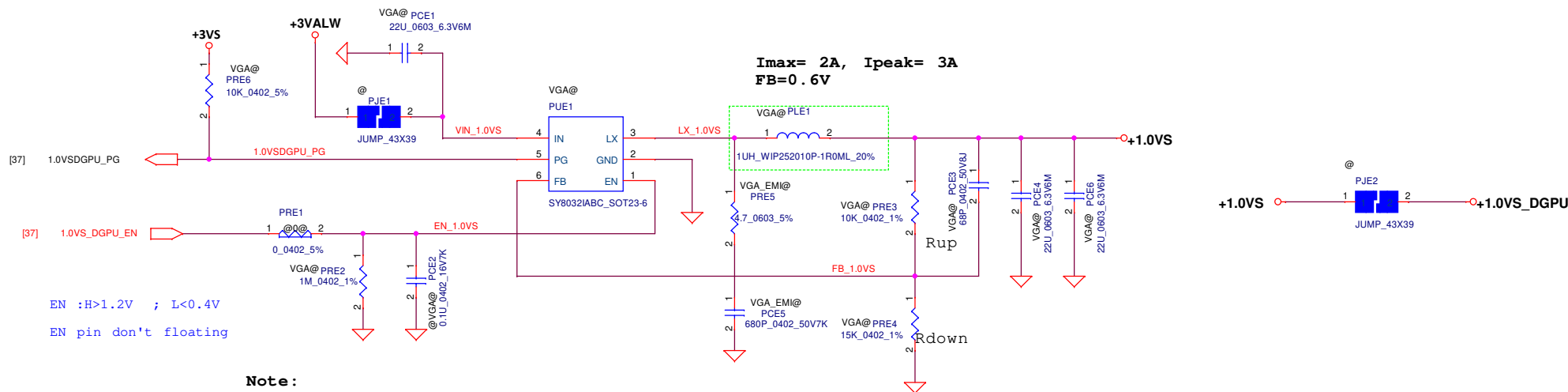


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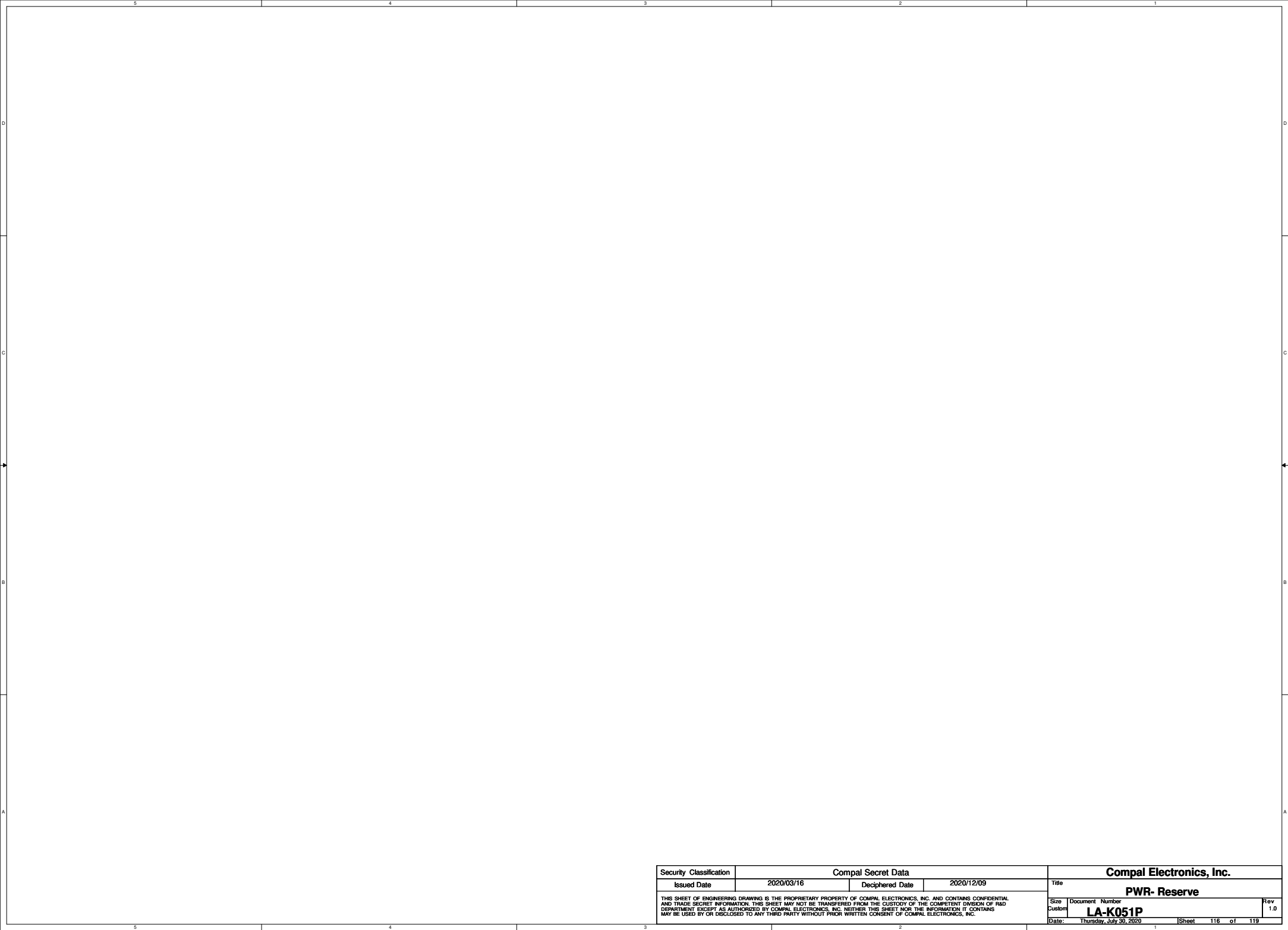
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Version change list (P.I.R. List)

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Item	Reason for change	PG#	Modify List	Date	Phase
1	Change +1.2VS solution	108	Modify related component and circuit	0316A	FVT
2	change +5VALW_USBC enable signal	88	Add PR520 and connect to 5V_EN	0316A	FVT
3	Adjust AOZ5038 FCCM voltage level	104	Add PRV128 pull-high to +5VALWand PRV129 pull-down to GND.	0316A	FVT
4	Adjust +1.2VS_VRAM enable voltage level	103	Change PRV118 from 100K to 10K	0316A	FVT
5	Modify by CPU transient test result	97	Change PRZ48 from 23.2K to 22.1K Change PRZ52 from 2.49K to 6.81K Change PRZ53 from 28.7K to 20.5K	0323A	FVT
6	Request to pop by RF	96 101	Change PCG37,PCG38,PCG39,PCG40,PCG41,PCG42 to pop Change PCZ60,PCZ61,PCZ65,PCZ181,PCZ182,PCZ183 to pop	0328A	FVT
7	Reserve for +VCCIN_AUX output cap	96	Reserve PCG35,PCG36,PCG43,PCG44 22u_0603_6.3V	0328A	FVT
8	Request to pop by EMI	98	Change PCZ20,PCZ56 to pop Change PRZ59,PRZ63 to pop Change PCZ49,PCZ64 to pop	0328A	FVT
9	For power consumption	103	Change VCC pin connect from "+5VALW" to "+5VS"	0328A	FVT
10	change to pop by EMI request	85 87 88	PRB14,PRB15,PCB20,PCB21,PR502,PC513,PR518,PC533 change to pop	0410A	FVT
11	To adjust current limit value to 16A	108	Change PRW37 from 0 to 1.18K Change PRW19 from 118K to 97.6K Change PRW20 from 11K to 9.09K Change PRW27 from 2.43K to 23.7K Change PRW24 from 240 to 3K	0416B	FVT
12	Request by HW	95	change VCCIN_AUX_CORE_VID0_R to VCCIN_AUX_CORE_VID0 change VCCIN_AUX_CORE_VID1_R to VCCIN_AUX_CORE_VID1	0416B	FVT_
13	Request by HW	108	change from "+1.35VGS_PGOOD" to "GPU_ALL_PGOOD"	0416B	FVT_
14	For test point adding requirement	88	change PR520 from 0402 to 0201 size	0416B	FVT_
15	To optimize SMT process	82 95 85 97 87 98	change from 0 ohm to short-pad : PR8,PRB4,PRB11,PRB32,PRB10,PRB12, PR511,PRG2,PRG5,PRG12,PRG14,PRG27,PRG30,PRG6,PRZ6,PRZ7,PRZ46, PRZ51,PRZ41,PRZ42,PRZ45,PRZ35,PRZ15,PRZ57,PRZ61	0416B	FVT_
16	To optimize SMT process	89 103 90 108 95 110 97	change from 0 ohm to short-pad : PRM3,PRM4,PR251,PR1804,PRG11,PRZ4,PRV10,PRW6,PRE1	0525A	SIT
17	NV request to smooth undershoot/overshoot during VID change	103	PCV16 change to 4700p	0525A	SIT
18	For sequence tuning	103	PCV20 change to unpop	0525A	SIT
19					
20					
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